General Description

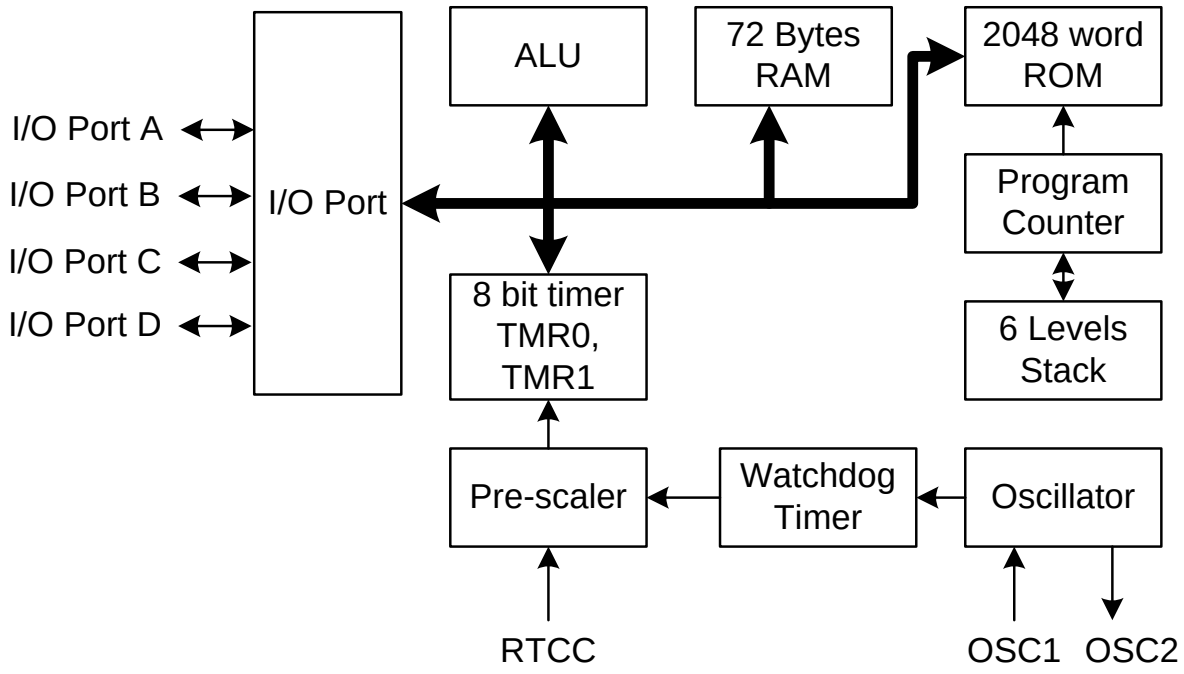
The MK6A20P is an 8 bit RISC high performance microcontroller. It has 2Kx14bits OTP(One Time Programmable) ROM, 72 Bytes RAM, Timer/Counter, Interrupt, LVR(Low Voltage Reset) and I/O ports in a single chip.

1. Feature

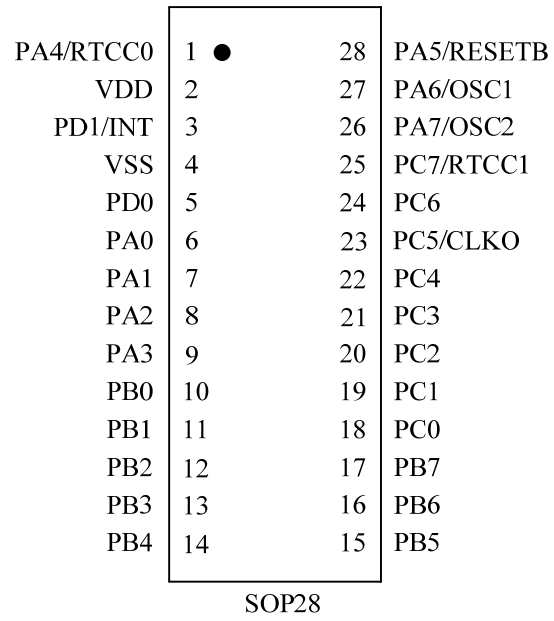
- ROM size: 2K x 14 bits
- RAM: 72 x 8 bits
- STACK: 6 Levels
- One instruction is built by 4 system clocks.
- 4 Reset modes:
  - Power-On reset
  - Low voltage reset
  - External RESETB
  - Watchdog timer count overflow reset
- 5 oscillation modes can be selected
  - External RC, LS (Low Speed) Crystal, NS (Normal Speed) Crystal and HS (High Speed) Crystal
  - Internal 4MHz RC oscillator
- 2 Timer/counters:
  - TMR0: 8 bit up count timer/counter with auto reload function
  - TMR1: 8 bit up count timer/counter with auto reload function
- Watchdog Timer: On chip WDT is based on an internal RC oscillator (for WDT used only). 8 periods can be selected. User can extend the WDT overflow period by using prescaler.
- 3 Interrupt events:
  - TMR0 Internal timer/event counter interrupt
  - TMR1 Internal timer/event counter interrupt
  - External Interrupt (INT)
- Up to 25 I/O pins and 1 input only pin:
  - PA0~7: 7 pins with individually programmable pull up, 1 input only pin (PA5)
  - PB0~7: 8 I/O pins with individually programmable pull up and pin change wakeup
  - PC0~7: 8 I/O pins with individually programmable pull up
  - PD0~1: 2 I/O pins with individually programmable pull up
- 3 Wake-up modes:
  A. Watch Dog timer wakeup
  B. Port B (PB0~7) pin change wakeup
  C. i_WDT wakeup

- Different Package Type:
  MK6A20PD28C: 28 pin SOP
  MK6A20PS28C: 28 pin SOP
  MK6A20PD20C: 20 pin DIP
  MK6A20PS20C: 20 pin SOP

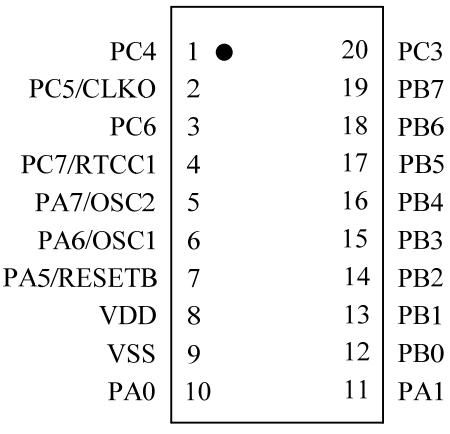
2. Block Diagram



3. Pin Definition & Pad Assignment



SOP28



PDIP20 / SOP20

4. Pin Description

Name	I/O	Description
PA0 ~ PA3	I/O	1. General purpose I/O port 2. Individually programmable pull high resistor
PA4/RTCC0	I/O	1. General purpose I/O port 2. Programmable pull high resistor 3. External clock input (for TMR0)
PA5/RESETB	I	1. Input pin only 2. System reset signal (active low)
PA6/OSC1	I/O	1. General purpose I/O port 2. Programmable pull high resistor 3. Oscillator input pin (DO NOT enable pull high resister in Crystal mode)
PA7/OSC2	I/O	1. General purpose I/O port 2. With pull high resistor . 3. Oscillator output pin (DO NOT enable pull high resister in Crystal mode)
PB0 ~ PB7	I/O	1. General purpose I/O port 2. Individually programmable pull high resistor 3. Individually programmable pin change wake up from sleep mode
PC0 ~ PC4	I/O	1. General purpose I/O port 2. With pull high resistor
PC5/CLKO	I/O	1. General purpose I/O port 2. Programmable pull high resistor 3. System clock output sys_c($13) b2=1.
PC6	I/O	1. General purpose I/O port 2. Programmable pull high resistor
PC7/RTCC1	I/O	1. General purpose I/O port 2. Programmable pull high resistor 3. External clock input (for TMR1).
PD0	I/O	1. General purpose I/O port 2. Programmable pull high resistor
PD1/INT	I/O	1. General purpose I/O port 2. Programmable pull high resistor 3. Programmable external interrupt triggered at rising edge

VDD	P	System Power Input
VSS	P	System Ground Input

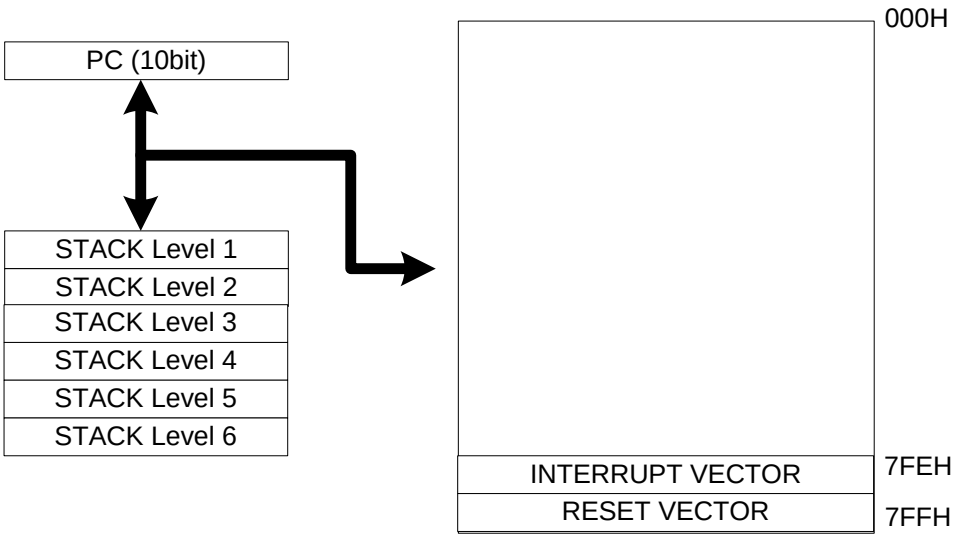
5. Memory Map

The MK6A20P has two kinds of memory which are program memory (ROM) and data memory. The program memory is used to store the program, table and interrupt vector with size of 2048x14bits. The data memory includes 20 bytes special purpose register and 72 bytes general-purpose RAM.

5.1 Program Memory (ROM)

Instruction and table are stored at this area. There is only one interrupt vector existed which means all the interrupt occurred would jump to the same vector. Programmer should use interrupt flag to judge what kind of interrupt is occurred. The program counter (PC) is 10 bit which can directly address all the 2048x14bits location. Look-up table can be put at anywhere of ROM.

The RESET vector is located at 7FFH and Interrupt vector is at 7FEH. The map is as below:



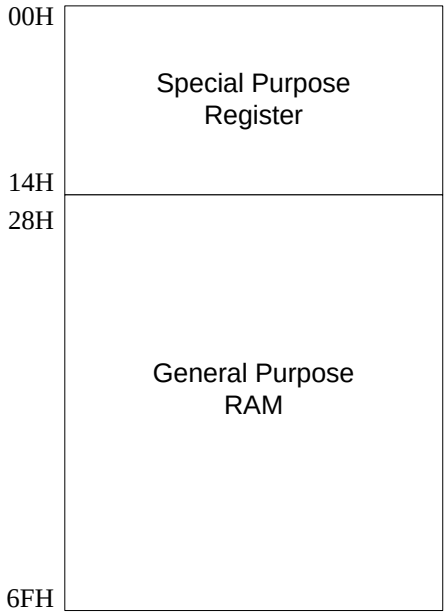
<Note> LCALL and LGOTO allow directly operate 2K word addressing

5.2 Data Memory (RAM)

The data memory includes two kinds of register group. One is 72 bytes general purpose RAM, the other is 20 bytes special purpose register.

The special purpose register is used to control specific function of this device. Detail description of those registers refers to the following chapter.

The data memory map is as below:



<Note> LCALL and LGOTO allow directly operate 2K word addressing

Special Purpose Register

Name	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CONFIGL	--	RESETE	LV	--	WDTE	CPT	INRC	FOSC1	FOSC0

Name	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CONFIGH	ADJ6	ADJ5	ADJ4	ADJ3	ADJ2	ADJ1	ADJ0	--	--

<Note> CONFIG is a 14 bit X 2 special register

Name	Addr	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IAR	$00	A7	A6	A5	A4	A3	A2	A1	A0
TM0_LA	$01	D7	D6	D5	D4	D3	D2	D1	D0
PCL	$02	A7	A6	A5	A4	A3	A2	A1	A0
STATUS	$03	--	BS1	BS0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
BSR	$04	1	D6	D5	D4	D3	D2	D1	D0
PA	$05	PA7	PA6	--	PA4	PA3	PA2	PA1	PA0
PB	$06	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0

PC	$07	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
PD	$08	--	--	--	--	--	--	PD1	PD0
IRQM	$09	INTM	--	--	--	--	EXINTM	TM1M	TM0M
IRQF	$0A	--	--	--	--	--	EXINTF	TM1F	TM0F
* PA_PUP	$0B	UA7	UA6	--	UA4	UA3	UA2	UA1	UA0
* PB_PUP	$0C	UB7	UB6	UB5	UB4	UB3	UB2	UB1	UB0
* PC_PUP	$0D	UC7	UC6	UC5	UC4	UC3	UC2	UC1	UC0
* PD_PUP	$0E	--	--	--	--	--	--	UD1	UD0
WAKEUP	$0F	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0
TM0_CTL	$10	TM0_EN	WR_CNT	SUR0	EDGE	PSA	PRE2	PRE1	PRE0
TM1_CTL	$12	TM1_EN	WR_CNT	SUR0	EDGE	--	PRE2	PRE1	PRE0
TM1_LA	$13	D7	D6	D5	D4	D3	D2	D1	D0
SYS_C	$14	i_WDT	i_STAB		EXINTE	--	CLK_OE	RTCE1	RTCE0

<Note1> "—" : mean no use.

" * " : mean write only .

<Note2> PA_PUP($0B), PB_PUP($0C), PC_PUP($0D), PD_PUP($0E) are write only register which can only use instructions below to write data :

MOVLA REG_Value

MOVAM PA_PUP

Configure Register

Name	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CONFIGL	--	RESETE	LV	--	WDTE	CPT	INRC	FOSC1	FOSC0

Name	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CONFIGH	ADJ6	ADJ5	ADJ4	ADJ3	ADJ2	ADJ1	ADJ0	--	--

CONFIG_H :

- Bit8~2 (ADJ6~0): Used to calibrated internal RC oscillator.

CONFIG_L :

- Bit7 (RESETE): RESETB pin define
  - 0: RESETB is normal input pin
  - 1: RESETB is system reset pin and triggered on negative pulse

- Bit6 (LV): Set voltage level of Low Voltage Reset (LVR)
  - 0: LVR = 3.7V

1: LVR = 2.1V (default)

- Bit4 (WDTE): Watchdog timer enable/disable
  0: WDT disable
  1: WDT enable

- Bit3 (CPT): ROM Code Protection bit
  0: ON
  1: OFF

- Bit2~0 (INRC, FOSC1~0): OSC type and system clock select

Bit2	Bit1	Bit0	OSC Type	Resonance Frequency
INRC	FOSC1	FOSC0		
0	0	0	LS (low speed)	System clock=32~200KHz
0	0	1	NS (Normal speed)	System clock=200K~10MHz
0	1	0	HS (high speed)	System clock=10~20MHz
0	1	1	External RC	System clock=32K ~ 10MHz
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Internal RC	System clock=4MHz

6. Function Deceptions

The function of this device consists of I/O ports, Timer, WDT, Interrupt, Table location, Reset, Program Counter and STATUS register. They will be described below in detail.

6.1 I/O Port

There are 4 I/O ports (portA, portB, portC and portD). All of the IOs are bidirectional general purpose I/O port with individually programmable pull up resistor, except PA5 is input only. The port B has pin wake up function. And some special function of those I/Os can also be programmed and activated.

6.1.1 Port A

A. PA ($05H):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PA	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0

- Bit 7~6 and Bit4~0 (PA7~6 and PA4~0): Data of I/O ports A
- Bit5 (PA5): Data input of PA5 (PA5/RESETB is set to normal input pin)

B. PA_PUP ($0BH):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PA_PUP	UA7	UA6	--	UA4	UA3	UA2	UA1	UA0

- Bit7~0 (UA7~0): Pull up resistor enables/disable

  0: Pull up resistor disable.

  1: Pull up resistor enable.

<Note> 1. PA5 is shared with RESETB and only can be used as input port.

PA6 and PA7 can only be used in RC oscillation mode. In Crystal mode, these two I/O are used to connect to the crystal and CANNOT be set to output or pull up enable. Otherwise, it will cause this device malfunction.

6.1.2 Port B

A. PB ($06H):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PB	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0

- Bit7~0 (PB7~0): Data of I/O Ports B

B. PB_PUP ($0CH):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PB_PUP	UB7	UB6	UB5	UB4	UB3	UB2	UB1	UB0

- Bit7~0 (UB7~0): Pull up resistor enable/disable.

  0: Pull up resistor disable.

  1: Pull up resistor enable.

6.1.3 Port C

A. PC ($07H):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PC	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0

- Bit7~0 (PB7~0): Data of I/O Ports B

B. PC_PUP ($0DH):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PC_PUP	UC7	UC6	UC5	UC4	UC3	UC2	UC1	UC0

- Bit7~0 (UC7~0): Pull up resistor enable/disable.

  0: Pull up resistor disable.

  1: Pull up resistor enable.

6.1.4 Port D

A. PD ($08H):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PD	--	--	--	--	--	--	PD1	PD0

- Bit1~0 (PD1~0): Data of I/O Ports D

B. PD_PUP ($0EH):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PD_PUP	--	--	--	--	--	--	UD1	UD0

- Bit1~0 (UD1~0): Pull up resistor enable/disable.
  0: Pull up resistor disable.
  1: Pull up resistor enable.

6.1.5 SYS_C ($14H):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SYS_C	i_WDT	i_STAB	--	EXTINTE	--	CLK_OE	RTCCE1	RTCCE0

- Bit7 : Internal Watch Dog Timer wakeup
  0: i_WDT mode disable (init)
  : i_WDT mode enable (WDTE must enable)
- Bit5: i_STAB (i_WDT mode) device stable time after wakeup from sleep
  0: 1.25ms (init)
  1: 625us (Lower power consumption)
- Bit4 : EXTINTE external interrupt function enable/ disable
  0: PD1 is general I/O
  1: PD1 is external interrupt pin (Rising Edge)
- Bit2 : CLK_OE system clock output function enable/ disable
  0: PC5 is general I/O
  1: PC5 is system clock output
- Bit1 : RTCCE1 TMR1 external clock input function enable/ dsiable
  0: PC7 is general I/O
  1: PC7 is TMR1 clock input

<Note> To use PC7 as counter RTCC1 input:

1. Set TMR1_CTL($12) SUR0(bit5) to 1.

2. Set RTCCE1 bit to 1 to set PC7 pin as RTCC and enable the RTCC clock in.

- Bit0 : RTCCE0 TMR0 external clock input function enable/ dsiable
  0: PA4 is general I/O

1: PA4 is TMR0 clock input

<Note> The method to count RTCC0 input are:

1. Set TMR0_CTL($10) SUR0(bit5) to 1.

2. Set RTCCE0 bit to 1 to set PA4 pin as RTCC and enable the RTCC clock in.

6.1.6 WAKEUP ($0FH):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WAKEUP	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0

- Bit7~0 (EN7~0): Port B pin change wakeup enable/disable

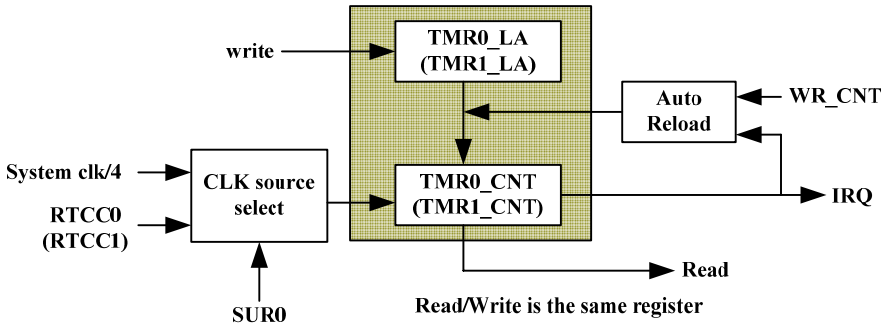
  0: Port B wakeup disable

  1: Port B wakeup enable

<Note> If i_WDT mode was enabled, bit 7(EN7) will be inhibited automatically.

6.2 Timers/Counters

The MK6A20P provides two up count timers/counters and 1 watchdog timer. Clock source of counters can be system clock or external clock by setting each timer control register. The detailed registers setting and block diagram are as below.



6.2.1. TMR0_CTL ($10H):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM0_CTL	TM0_EN	WR_CNT	SUR0	EDGE	PSA	PRE2	PRE1	PRE0

- Bit7 : (TM0_EN) Timer0 enable/disable

  0: disable

  1: enable

- Bit6 : (WR_CNT) Auto pre_load TMR0 data

  0: disable

  1: enable

- Bit5 : (SUR0) TMR0 clock source select

  0: system clock / 4 (1 instruction cycle)

  1: external clock input (PA4/RTCC0)

- Bit4 : (EDGE) TMR0 external clock edge control bit

  0 : increment when L→H transition on external clock

  1 : increment when H→L transition on external clock

- Bit3 : (PSA) Prescaler assignment bit

  0: Prescaler assigned to TMR0

  1: Prescaler assigned to WDT

- Bit2~0 (PRE2~0): Set TM0(WDT) prescaler rate

Bit2	Bit1	Bit0	TM0 Prescaler rate	WDT Prescaler rate
PRE2	PRE1	PRE0		
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

6.2.2. TMR0_LA ($01H):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM0_LA	D7	D6	D5	D4	D3	D2	D1	D0

- Bit7~0 : (TM0_LA) Timer0 Data

<Note> This timer is a up count timer. When it up counts from 0xff to 00, the counter overflow will occur and the flag (TM0F) will be set to "1". At this moment, the zero flag will not be affected. Please read TM0F to judge whether it overflow or not.

6.2.3. TMR1_CTL ($12H):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM1_CTL	TM1_EN	WR_CNT	SUR0	EDGE	--	PRE2	PRE1	PRE0

- Bit7 : (TM1_EN) Timer1 enable/disable

  0: disable

  1: enable

- Bit6 : (WR_CNT) Auto pre_load TMR1 data

  0: disable

  1: enable

- Bit5 : (SUR0) TMR1 clock source select

  0: system clk / 4 (1 instruction cycle)

1: external clock input (PC7/RTCC1)

- Bit4 : (EDGE) TMR1 external clock edge control bit

  0 : increment when L→H transition on external clock

  1 : increment when H→L transition on external clock

- Bit2~0 (PRE2~0): Set TM1 prescaler rate

Bit2	Bit1	Bit0	TM1 Prescaler rate
PRE2	PRE1	PRE0	
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.2.4. TMR1_LA ($13H):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM1_LA	D7	D6	D5	D4	D3	D2	D1	D0

- Bit7~0 : (TM1_LA) Timer1 Data

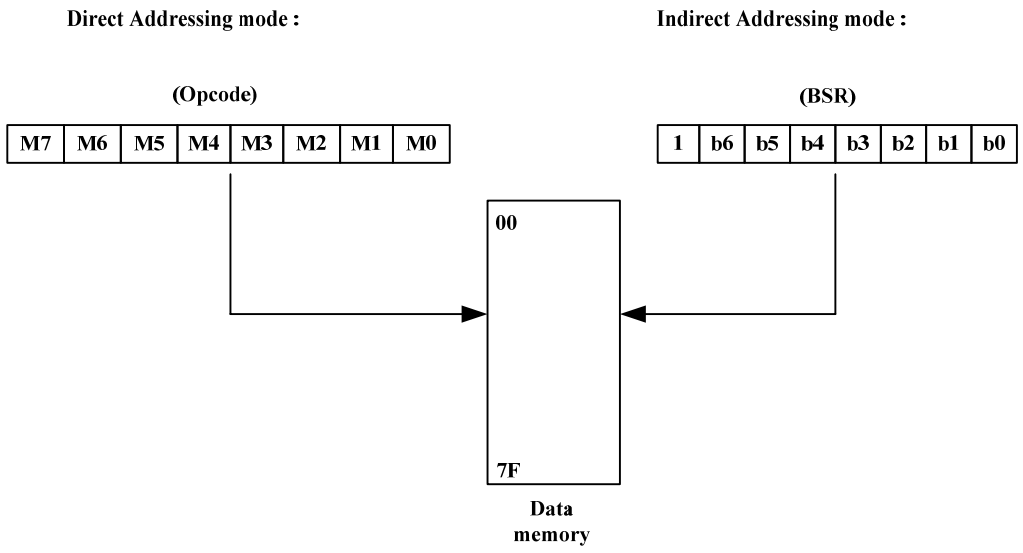
<Note> This timer is a up count timer. When it up counts from 0xff to 0x 00, the counter overflow will occur and the flag (TM1F) will be set to "1". At this moment, the zero flag will not be affected. Please read TM1F to judge whether it overflow or not.

```
MOVLA     b'10000001'
MOVAM     IRQM ; set tm0 irq enable ;
CLR       IRQF ; clear tm0 flag ;
MOVLA     b'01000010'
MOVAM     TMR0_CTL ; bit6=1; auto pre_load, bit5=0; clk=system clk/4,
                   ;Bit3=0; pre-scaler assign to tm0, pre-scaler=1:8
MOVLA     b'10000000'
MOVAM     TMR0_LA
BS        TMR0_CTL,7 ; tm0 start = inrc(4mhz)/4 x 8 x 128=1024us ;
  .
  .
  .
```

```
        .
INT:
        MOVLA       0XFE
        MOVAM       IRQF ; clear tm0 flag ;
        .
        .
        .
        .
        RETI
```

6.3 Indirect Addressing

Register IAR($00) and BSR($04) will be used to address indirectly. BSR (Bank Select Register) allows 7-bit wide operand to directly access the whole data (00~7F) data memory. The method is as below map:



6.4 WDT (Watchdog Timer)

WDT is a timer to prevent software from malfunction or jumping to an unknown location with unpredictable result. The source clock of WDT is an independent internal RC oscillator. This timer would be affected by temperature, voltage and different production lot. The minimum time is around 20ms. Programmer can use TM0_CTL(bit3) to set prescaler and get the different duration. Since WDT and TM0 share this prescale, only one can use this prescaler at a time.

6.5 Reset

There are 4 events will cause reset which is listed as below. The power-down event will cause MK6A20P reset. This is used to protect chip in deficient power environment. The last two cases are called warm reset. Different reset events will affect registers and RAM. The $\overline{TO}$ and $\overline{PD}$ bits can be used to determine the type of reset, please refer to section 6.5.2.

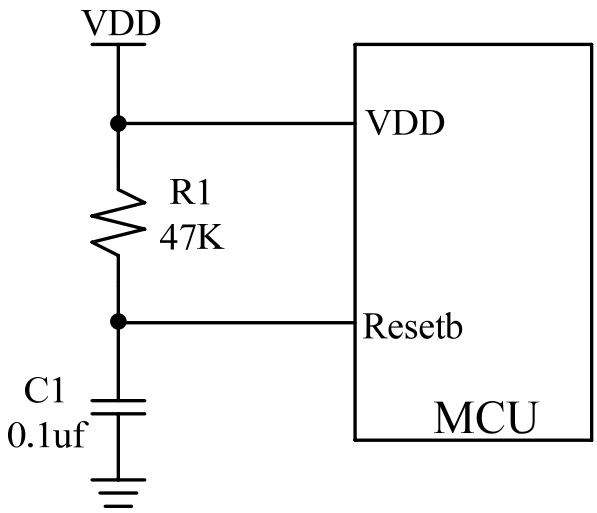
(1) Power-on reset.

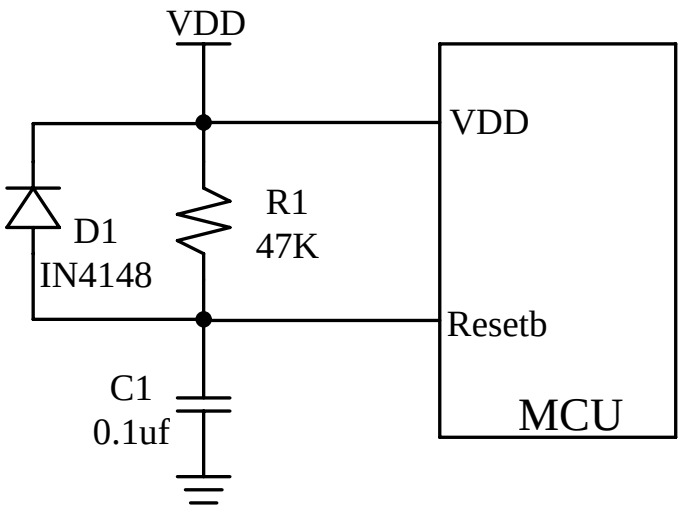
(2) Low voltage reset (LVR).

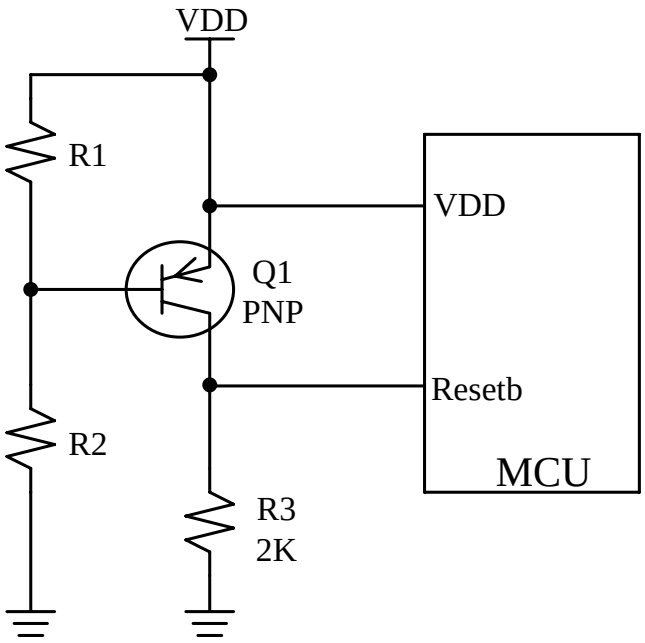
(3) RESETB pin reset (input a negative pulse).

(4) WDT timer overflow reset.

6.5.1 External Reset Circuit



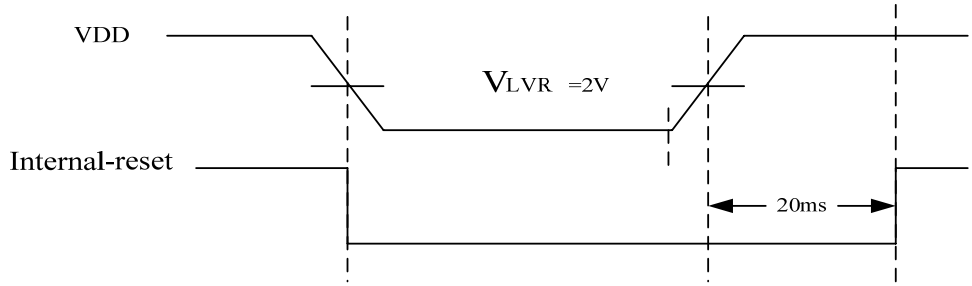




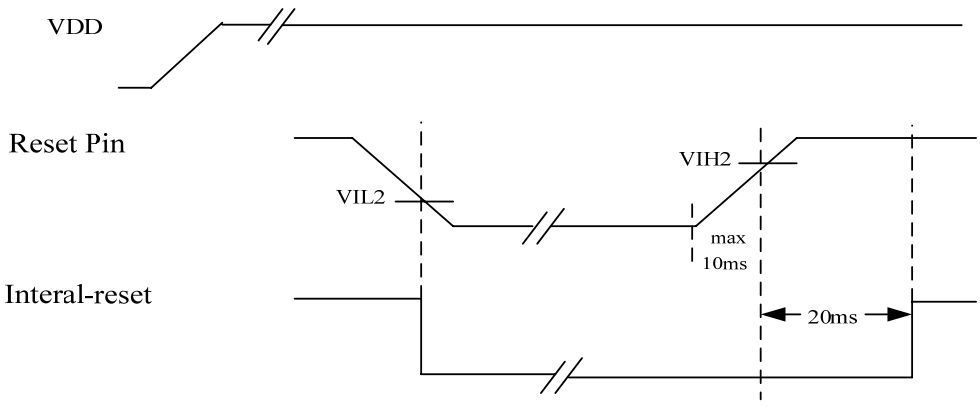
VDD Voltage level is above or equal to " 0.7V x (R1 + R 2) / R1 " , Resetb pin is High and MCU Operates normally . When VDD is below " 0.7V x (R1 + R 2) / R1 " Resetb pin is low and MCU Is in reset mode .

Timming :

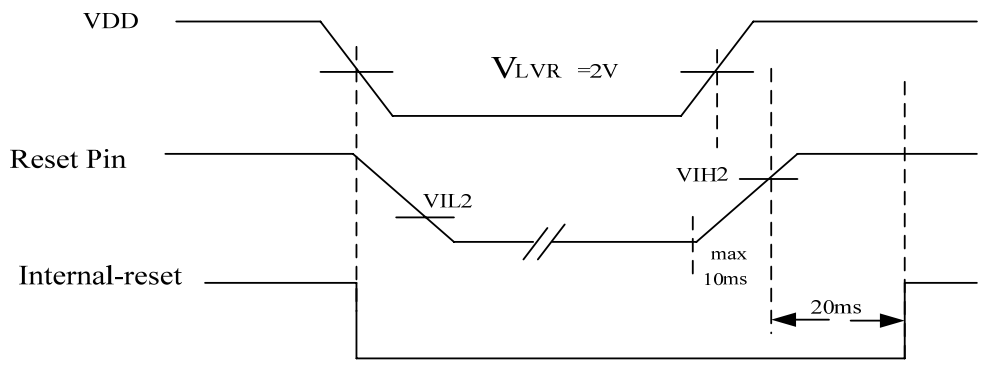
1. LVR on / RESET Disable



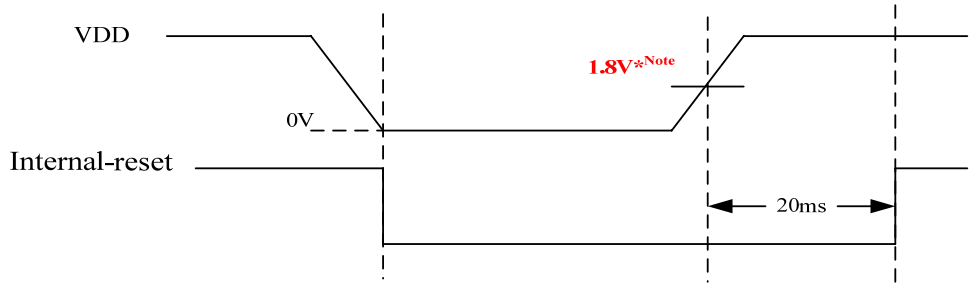
2. LVR off /RESET Enable



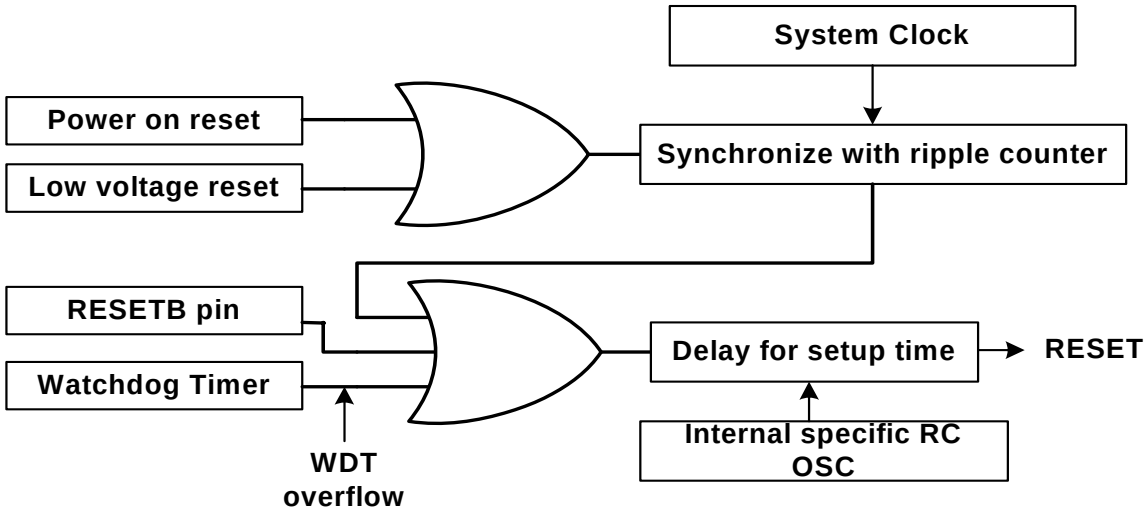
3. LVR on / RESET Enable



4. LVR off / RESET Disable



Note: This 1.8V may be variant during IC fabrication and device application environment.



System Reset Block

<Note>: the watchdog setup time is approximately 20ms that will have some tolerance due to power voltage, process and temperature variations.

Address	Name		Cold Reset	Warm Reset
N/A	Accumulator		xxxx xxxx	pppp pppp
N/A	IODIR	PA	1111 1111	1111 1111
		PB	1111 1111	1111 1111
		PC	1111 1111	1111 1111
		PD	xxxx xx11	xxxx xx11
00h	IAR		---- ----	---- ----
01h	TM0_LA		0000 0000	0000 0000
02h	PCL		11 1111 1111	11 1111 1111
03h	STATUS		0001 1xxx	#00# #ppp
04h	BSR		1xxx xxxx	1ppp pppp
05h	PA		xxxx xxxx	ppxp pppp
06h	PB		xxxx xxxx	pppp pppp
07h	PC		xxxx xxxx	pppp pppp
08h	PD		xxxx xxxx	xxxx xxpp
09h	IRQM		0000 0000	0000 0000
0Ah	IRQF		0000 0000	0000 0000
0Bh	PA_PUP		00x0 0000	00x0 0000
0Ch	PB_PUP		0000 0000	0000 0000
0Dh	PC_PUP		0000 0000	0000 0000
0Eh	PD_PUP		0000 0000	0000 0000
0Fh	WAKEUP		0000 0000	0000 0000
10h	TM0_CTL		0110 0000	0110 0000
12h	TM1_CTL		0000 0000	0000 0000
13h	TM1_LA		0000 0000	0000 0000
14h	SYS_C		00x0 x000	00x0 x000
28h~6Fh	General Purpose RAM		xxxx xxxx	pppp pppp

<Note> x: unknown; p: keep as previous data ; #: value depends on condition

-:unimplemented and read as"0".

6.5.2 Reset condition of STATUS register

Condition	Status Register	
	$\overline{TO}$	$\overline{PD}$
1.Power-on reset	1	1
2.RESETB reset during normal operation	U	U
3.RESETB reset during sleep	1	0
4.WDT reset during sleep<Note 1>	0	0
5.WDT reset during normal operation<Note 1>	0	1
6.Wake up by pin changed	1	0

<Note> 1. If the CLRWDT instruction been executed before, the content of item 4/5 would become"11" the same as item 1.

2. U: Unchanged

6.6 Interrupt

The MK6A20P provides 3 interrupts which are TM0, TM1 and external INT. IRQM and IRQF registers are used to control or declare request state of all interrupts. IRQM is used to enable/disable interrupt and IRQF is used to indicate which interrupt is occurred. If the specific IRQM doesn't enable then the hardware interrupt would not occurred. But the IRQF will response the status no matter how IRQM enable or not. For example, TMR0 is enabled and start counting. If IRQM bit 0 is enabled, the hardware interrupt would generate when timer overflow and IRQF bit 1 will be set. At the same time, program will jump to interrupt vector. IRQF should be cleared in interrupt service routine, otherwise the interrupt would not work properly. Another condition is if IRQM bit 0 is disabled, the interrupt would not generate when timer overflow, but IRQF bit 1 will still be set, but the program would not jump to interrupt vector.

A. IRQM ($09H)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRQM	INTM	--	--	--	--	EXINTM	TM1M	TM0M

- Bit7 (INTM): Global interrupt enable bit.

  0: Disable. All interrupts are masked.

  1: Enable. All interrupt are unmasked

  When interrupt is serving, the INTM will be set to "0" to prevent the other interrupt happen. After interrupt service routine, the RETI instruction will set INTM to '1'.

- Bit2 (EXTINTM): external interrupt (PD1/INT) enable/disable

  0: Disable Interrupt

  1: Enable Interrupt

- Bit1 (TM1M): TM1 interrupt enable/disable
  0: Disable Interrupt
  1: Enable Interrupt
- Bit0 (TM0M): TM0 interrupt enable/disable
  0: Disable Interrupt
  1: Enable Interrupt

B. IRQF ($0AH)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRQF	--	--	--	--	--	EXINTF	TM1F	TM0F

- Bit2 (EXINTF): external interrupt (PD1/INT) flag
  0: External interrupt doesn't occur
  1: Extrernal interrupt signal occurred
- Bit1 (TM1F): TM1 interrupt flag
  0: Interrupt signal doesn't occur
  1: Interrupt signal occurred
- Bit0 (TM0F): TM0 interrupt flag
  0: Interrupt signal doesn't occur
  1: Interrupt signal occurred

Note : If those interrupts used, please do not use " BC " instruction to clear those flags .

Please use the following instrunction instead:

```
MOVLA     0XFE
MOVAM     IRQF    ; clear TM0F (IRQF,0) ;
```

6.7 STATUS Register

The STATUS register is an 8-bit register that contains the zero flag (Z), carry flag (C), Nibble carry flag (DC), power down flag ($\overline{PD}$), and watchdog timer overflow flag ($\overline{TO}$). It records the status information of this device.

A. STATUS($03H)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STATUS	**--**	**BS1**	**BS0**	$\overline{TO}$	$\overline{PD}$	**Z**	**DC**	**C**

- Bit6~5 (BS1,BS0) : ROM bank select
  0 0 (init) : Bank0 (000H ~ 0FFH).
  0 1 : Bank1 (200H ~ 2FFH).
  1 0 : Bank2 (400H ~ 4FFH).
  1 1 : Bank3 (600H ~ 6FFH)

Table Example 1: LGOTO with PCL register calculation on Bank0 (BS1,BS0=00)

```
        ORG 000H :
                BC          STATUS,5
                BC          STATUA,6 ; set ROM bank = 000h ~ 0FFh ;
                MOVLA       0X00
                LCALL       TABLE

                ……..
TAB1
                ….. RET
TAB2
                ….. RET
TAB3
                ….. RET

        ORG 0F0H :
TABLE
                ADD         PCL,m       ; PCL register calculation
                LGOTO       TAB1 ; Acc=0 ;  Program can only jump within Bank0
                LGOTO       TAB2 ; Acc=1 ;
                LGOTO       TAB2 ; Acc=2 ;
```

Table Example 2: LGOTO with PCL register calculation on Bank1 (BS1,BS0=01)

```
        ORG 000H :
                BC          STATUS,5
                BS          STATUA,6 ; set ROM bank = 200h ~ 2FFh ;
                MOVLA       0X00
                LCALL       TABLE


        ORG 200H :
TAB1
                …..RET
TAB2
                ….. RET
```

```
TAB3
            ….. RET

TABLE
            ADD     PCL,m       ; PCL register calculation
            LGOTO   TAB1 ; Acc=0 ; ; Program can only jump within Bank1
            LGOTO   TAB2 ; Acc=1 ;
            LGOTO   TAB2 ; Acc=2 ;
```

Table Example 3: RETLA with PCL register calculation on Bank0 (BS1,BS0=00)

```
    ORG 000H :
            BC      STATUS,5
            BC      STATUA,6 ; set ROM bank = 000h ~ 0FFh ;
            MOVLA   0X00
            LCALL   TABLE

    ORG 0F0H :
TABLE
            ADD     PCL,m
            RETLA   0XAA  ; Acc=AA ;
            RETLA   0XAB  ; Acc=AB ;
            RETLA   0XAC  ; Acc=AC ;
```

Table Example 4: RETLA with PCL register calculation on Bank1 (BS1,BS0=01)

```
    ORG 000H :
            BC      STATUS,5
            BS      STATUA,6 ; set ROM bank = 200h ~ 2FFh ;
            MOVLA   0X00
            LCALL   TABLE

    ORG 200H :
TABLE
            ADD     PCL,m
            RETLA   0XAA  ; Acc=AA ;
            RETLA   0XAB  ; Acc=AB ;
            RETLA   0XAC  ; Acc=AC ;
```

- Bit4 ($\overline{TO}$): Watchdog Timer overflow flag bit
- Bit3 ($\overline{PD}$):Power down flag bit

$\overline{TO}$	$\overline{PD}$	Description
0	0	WDT timer overflow from sleep mode
0	1	WDT timer overflow from normal mode
1	0	Input a 'low" at RESETB from sleep mode
1	1	Power on reset
Unchanged	Unchanged	Input a "low" at RESETB from normal mode

- Bit2 (Z): zero flag bit

  0: the result of a logic operation is not zero

  1: the result of a logic operation is zero

- Bit1 (DC): Nibble Carry and Nibble $\overline{Borrow}$ flag bit

  ADD instruction:

  0: no carry

  1: a carry from the low nibble bits of the result occurred

  SUB instruction

  0: a borrow from the low nibble bits of the result occurred

  1: no borrow

- Bit0 (C): Carry and $\overline{Borrow}$ flag bit

  ADD instruction:

  0: no carry

  1: a carry occurred from the MSB

  SUB instruction

  0: a borrow occurred from the MSB

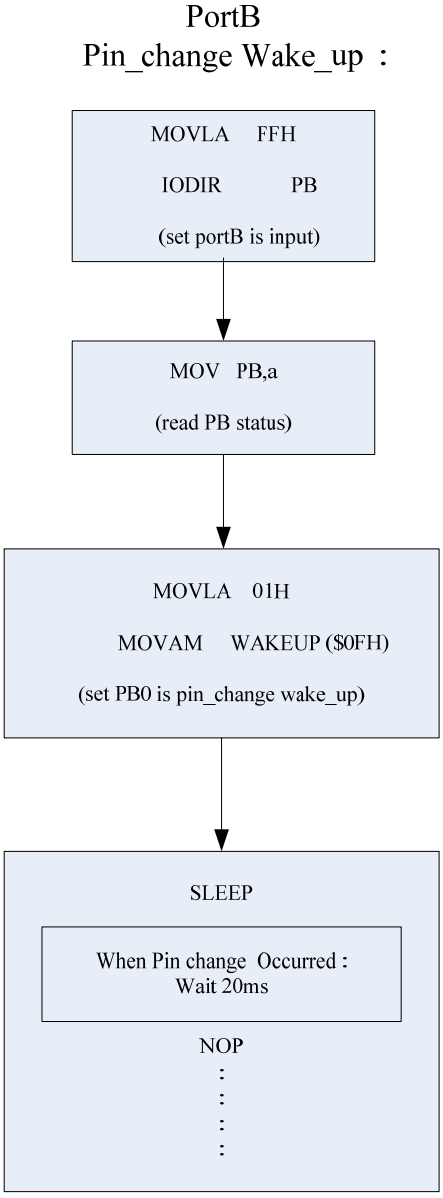
  1: no borrow

6.8 Wake up function

6.8.1 pin change wake_up

The chip provide pin signal toggle wake up function. It will wake up from sleep mode when selected I/O signal toggled. In order to safely wake up from sleep mode, reading the input pin to store data before entering sleep mode will be recommended. The sample program is as below:

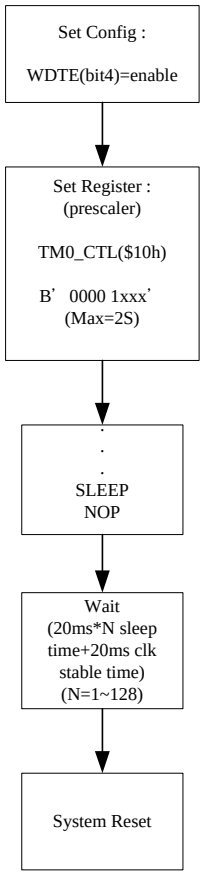
```
MOVLA     FFh
IODIR     PB          ;// set bit0~7 of port B as input. Only input pin can be wake up
……        ……..
MOV       PB,a        ;//Store the data of input pin before sleep
BS        WAKEUP,0    ;//Set PB0 is wakeup pin
SLEEP                 ;// if doesn't perform the read instruction, then can not enter
                      ;// SLEEP mode
NOP                   ;//Add NOP instruction to delay a while for system stability
```



6.8.2 i_WDT wake_up

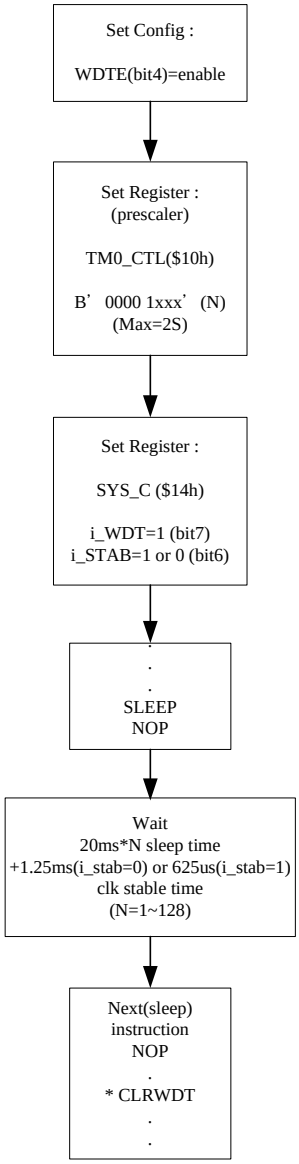
The chip provide internal watch dog (i_WDT) wake up function. It will return from sleep mode when watch dog timer overflow without triggering device reset. In order to safely wake up from sleep mode, this wake up mode must set the config bit WDTE(bit4) enable, and the register SYS_C ($14h) i_WDT(bit7) to 1. At this stage, bit 7 (EN7) of register WAKEUP ($0FH) will be inhibited. The setting flow of i_WDT is as below:

WDT-Wakeup :
(Watch-dog timer wake-up)




```
start
        clrwdt
        movla    0Fh
        movam    tm0_ctl    ;set prescaler
                              for WDT
                              & prescaler=128
          .
          .
          .
        Sleep
        nop
System reset
```

i_WDT-Wakeup :
(Internal watch-dog timer
wake-up)



*When wakeup must CLRWDT, otherwise watch-dog timer will keep operation

```
start
        clrwdt
        movla    0fh
        movam    tm0_ctl    ;set prescaler
                              for WDT
          .                   & prescaler=128
          .
          .
        Sleep
        nop
        clrwdt
          .
          .
          .
```

Instruction

<Note> Instruction cycle is system clock/4

Mnemonic Operands	Instruction Code (Advance)	Cycles	Status Affected	**OP-code**
ADD M, m	(M)+(acc) → (M)	1	C, DC, Z	01 0101 1MMM MMMM
ADD M, a	(M)+(acc) → (acc)	1	C, DC, Z	01 0101 0MMM MMMM
AND M, m	(M) · (acc) → (M)	1	Z	01 0100 1MMM MMMM
AND M, a	(M) · (acc) → (acc)	1	Z	01 0100 0MMM MMMM
ANDLA I	Literal · (acc) → (acc)	1	Z	11 1001 iiii iiii
BC M, b0	Clear bit0 of (M)	1	None	00 1100 0MMM MMMM
BC M, b1	Clear bit1 of (M)	1	None	00 1100 1MMM MMMM
BC M, b2	Clear bit2 of (M)	1	None	00 1101 0MMM MMMM
BC M, b3	Clear bit3 of (M)	1	None	00 1101 1MMM MMMM
BC M, b4	Clear bit4 of (M)	1	None	00 1110 0MMM MMMM
BC M, b5	Clear bit5 of (M)	1	None	00 1110 1MMM MMMM
BC M, b6	Clear bit6 of (M)	1	None	00 1111 0MMM MMMM
BC M, b7	Clear bit7 of (M)	1	None	00 1111 1MMM MMMM
BS M, b0	Set bit0 of (M)	1	None	00 1000 0MMM MMMM
BS M, b1	Set bit1 of (M)	1	None	00 1000 1MMM MMMM
BS M, b2	Set bit2 of (M)	1	None	00 1001 0MMM MMMM
BS M, b3	Set bit3 of (M)	1	None	00 1001 1MMM MMMM
BS M, b4	Set bit4 of (M)	1	None	00 1010 0MMM MMMM
BS M, b5	Set bit5 of (M)	1	None	00 1010 1MMM MMMM
BS M, b6	Set bit6 of (M)	1	None	00 1011 0MMM MMMM
BS M, b7	Set bit7 of (M)	1	None	00 1011 1MMM MMMM
BTSC M, b0	If bit0 of (M) = 0, skip next instruction	1 + (skip)	None	00 0100 0MMM MMMM
BTSC M, b1	If bit1 of (M) = 0, skip next instruction	1 + (skip)	None	00 0100 1MMM MMMM
BTSC M, b2	If bit2 of (M) = 0, skip next instruction	1 + (skip)	None	00 0101 0MMM MMMM
BTSC M, b3	If bit3 of (M) = 0, skip next instruction	1 + (skip)	None	00 0101 1MMM MMMM
BTSC M, b4	If bit4 of (M) = 0, skip next instruction	1 + (skip)	None	00 0110 0MMM MMMM
BTSC M, b5	If bit5 of (M) = 0, skip next instruction	1 + (skip)	None	00 0110 1MMM MMMM

BTSC M, b6	If bit6 of (M) = 0, skip next instruction	1 + (skip)	None	00 0111 0MMM MMMM
BTSC M, b7	If bit7 of (M) = 0, skip next instruction	1 + (skip)	None	00 0111 1MMM MMMM
BTSS M, b0	If bit0 of (M) = 1, skip next instruction	1 + (skip)	None	00 0000 0MMM MMMM
BTSS M, b1	If bit1 of (M) = 1, skip next instruction	1 + (skip)	None	00 0000 1MMM MMMM
BTSS M, b2	If bit2 of (M) = 1, skip next instruction	1 + (skip)	None	00 0001 0MMM MMMM
BTSS M, b3	If bit3 of (M) = 1, skip next instruction	1 + (skip)	None	00 0001 1MMM MMMM
BTSS M, b4	If bit4 of (M) = 1, skip next instruction	1 + (skip)	None	00 0010 0MMM MMMM
BTSS M, b5	If bit5 of (M) = 1, skip next instruction	1 + (skip)	None	00 0010 1MMM MMMM
BTSS M, b6	If bit6 of (M) = 1, skip next instruction	1 + (skip)	None	00 0011 0MMM MMMM
BTSS M, b7	If bit7 of (M) = 1, skip next instruction	1 + (skip)	None	00 0011 1MMM MMMM
CLRA	Clear accumulator	1	Z	01 0001 0000 0000
CLR M	Clear memory M	1	Z	01 0001 1MMM MMMM
CLRWDT	Clear watch-dog register	1	TO, PO	01 0000 0000 0001
COM M, m	~(M) → (M)	1	Z	01 0010 1MMM MMMM
COM M, a	~(M) → (acc)	1	Z	01 0010 0MMM MMMM
DEC M, m	Decrement M to M	1	Z	01 0110 1MMM MMMM
DEC M, a	(M) - 1 → (acc)	1	Z	01 0110 0MMM MMMM
DECSZ M, m	(M) - 1 → (M), skip if (M) = 0	1 + (skip)	None	01 0111 1MMM MMMM
DECSZ M, a	(M) - 1 → (acc), skip if (M) = 0	1 + (skip)	None	01 0111 0MMM MMMM
INC M, m	(M) + 1 → (M)	1	Z	01 1000 1MMM MMMM
INC M, a	(M) + 1 → (acc)	1	Z	01 1000 0MMM MMMM
INCSZ M, m	(M) + 1 → (M), skip if (M) = 0	1 + (skip)	None	01 1001 1MMM MMMM
INCSZ M, a	(M) + 1 → (acc), skip if (M) = 0	1 + (skip)	None	01 1001 0MMM MMMM
IODIR M	Set i/o direction	1	None	01 0000 0000 MMMM
IOR M, m	(M) ior (acc) → (M)	1	Z	01 1111 1MMM MMMM
IOR M, a	(M) ior (acc) → (acc)	1	Z	01 1111 0MMM MMMM
IORLA I	Literal ior (acc) → (acc)	1	Z	11 0011 iiii iiii
LCALL I	Call subroutine. However, LCALL can addressing 1K address	2	None	10 0iii iiii iiii
LGOTO I	Go branch to any address	2	None	10 1iii iiii iiii

MOVAM m	Move data form acc to memory	1	None	01 0000 1MMM MMMM
MOVLA I	Move literal to accumulator	1	None	11 0001 iiii iiii
MOV M, m	(M) → (M)	1	Z	01 0011 1MMM MMMM
MOV M, a	(M) → (acc)	1	Z	01 0011 0MMM MMMM
NOP	No operation	1	None	01 0000 0000 0000
RET	Return	2	None	11 1111 0111 1111
RETI	Return and enable INTM	2	None	11 1111 1111 1111
RETLA I	Return and move literal to accumulator	2	None	11 1100 iiii iiii
RL M, m	Rotate left from m to itself	1	C	01 1100 1MMM MMMM
RL M, a	Rotate left from m to acc	1	C	01 1100 0MMM MMMM
RR M, m	Rotate right from m to itself	1	C	01 1110 1MMM MMMM
RR M, a	Rotate right from m to acc	1	C	01 1110 0MMM MMMM
SLEEP	Enter sleep (saving) mode	1	TO, PO	01 0000 0000 0011
SUB M, m	(M)–(acc) → (M)	1	C, DC, Z	01 1010 1MMM MMMM
SUB M, a	(M) –(acc) → (acc)	1	C, DC, Z	01 1010 0MMM MMMM
SWAP M, m	Swap data from m to itself	1	None	01 1101 1MMM MMMM
SWAP M, a	Swap data from m to acc	1	None	01 1101 0MMM MMMM
XOR M, m	(M) xor (acc) → (M)	1	Z	01 1011 1MMM MMMM
XOR M, a	(M) xor (acc) → (acc)	1	Z	01 1011 0MMM MMMM
XORLA I	Literal xor (acc) → (acc)	1	Z	11 1000 iiii iiii

<Note> After SLEEP instruction, please add a NOP instruction to perform transient.

7. Electrical Characteristics

7.1 Absolute Maximum Ratings

Supply Voltage …. Vss-0.3V to Vss+5.5V Storage Temperature ……. –40℃ to 125℃

Input Voltage …… Vss-0.3V to VDD+0.3V Operating Temperature ….. –40℃ to 70℃

7.2 DC Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		VDD	Conditions				
VDD	Operating Voltage	---		2.2		5.5	V
V_{por}	V_{dd} rise rate	--	Vdd rise rate to ensure internal power on reset	0.1			V/ms
V_{IH1}	Input HighVoltage	--	I/O Port	0.6VDD		VDD	V
V_{IL1}	Input Low Voltage	--	I/O Port	0		0.25VDD	V
V_{IH2}	Input HighVoltage	--	Reset Pin (PA5)	0.7VDD		VDD	V
V_{IL2}	Input Low Voltage	--	Reset Pin (PA5)	0		0.2VDD	V
I_{DD1}	Standby Current	5V	WDT disable,(LV ON)			3	μA
			WDT disable,(LV OFF)			1	
			WDT enable,(LV ON)			11	
			WDT enable, (LV OFF)			9	
		3V	WDT disable,(LV ON)			1	
			WDT disable,(LV OFF)			1	
			WDT enable,(LV ON)			2	
			WDT enable,(LV OFF)			2	
I_{DD1}	operating current	5V	reset=hi, Fosc=4MHZ, No Load		2		mA
I_{IL}	Input Leakage Current	5V	Vin=VDD, VSS			1	μA
I_{OH}	output high driving current	5V	Voh=0.9V_{DD}		-9		mA
		3V	Voh=0.9V_{DD}		-4		mA

I_{OL}	output low sink current	5V	Vol=0.1V_{DD}		20		mA
		3V	Vol=0.1V_{DD}		8		mA
V_{LV1}	Low Voltage reset (LVR=2.1V)		Ta = 25℃	1.9	2.1	2.3	V
V_{LV2}	Low Voltage reset (LVR=3.7V)		Ta = 25℃	3.5	3.7	3.9	V

7.3 AC Characteristics

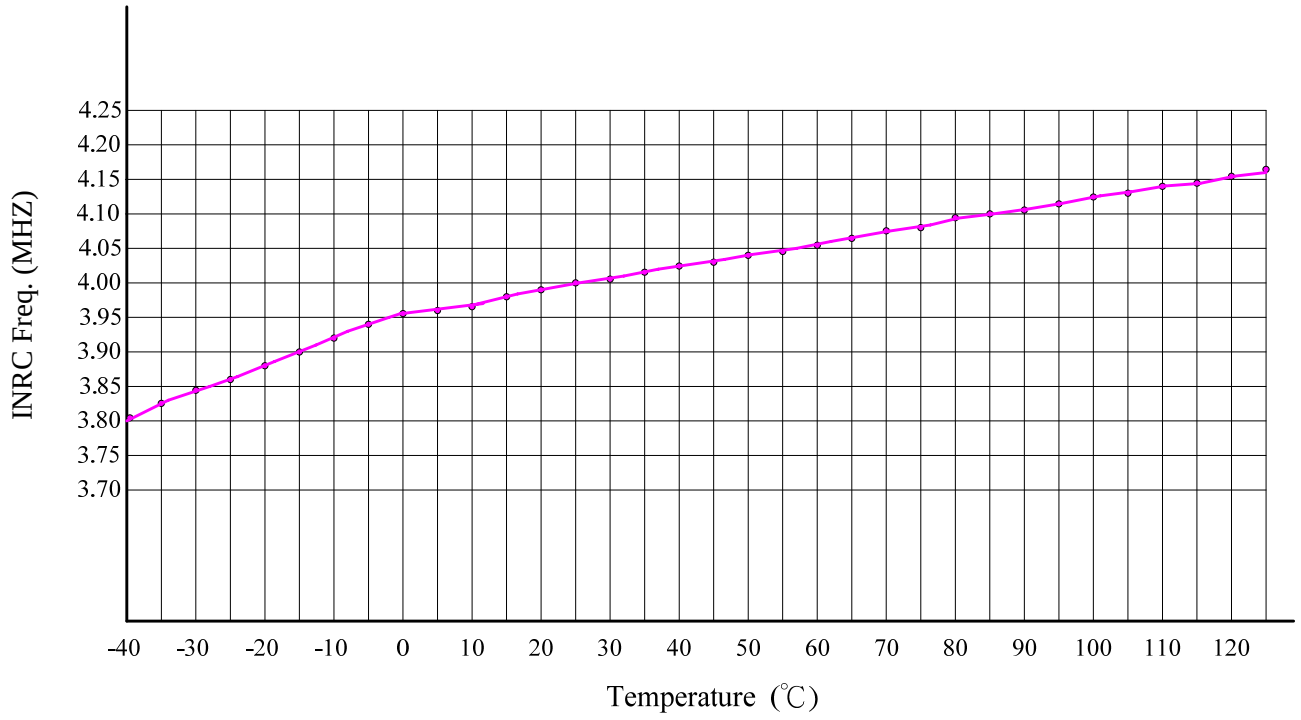
Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
		Conditions	VDD				
f_{sys1}	System Clock	LP Crystal mode	5V	32		200	Khz
			3V	32		200	
f_{sys2}	System Clock	NT Crystal mode	5V	0.2		10	Mhz
			3V	0.2		10	
f_{sys3}	System Clock	HS Crystal mode	5V	10		20	Mhz
f_{sys4}	System Clock	RC mode	5V	3.4	4	4.6	Mhz
			3V	3.4	4	4.6	
T_{wdt}	Watchdog Timer		5V		20		MS
			3V		24		MS

7.4 Internal 4MHZ RC Temperature Characteristic

Power Voltage (VDD) = 5V

Typical Temperature = 25℃

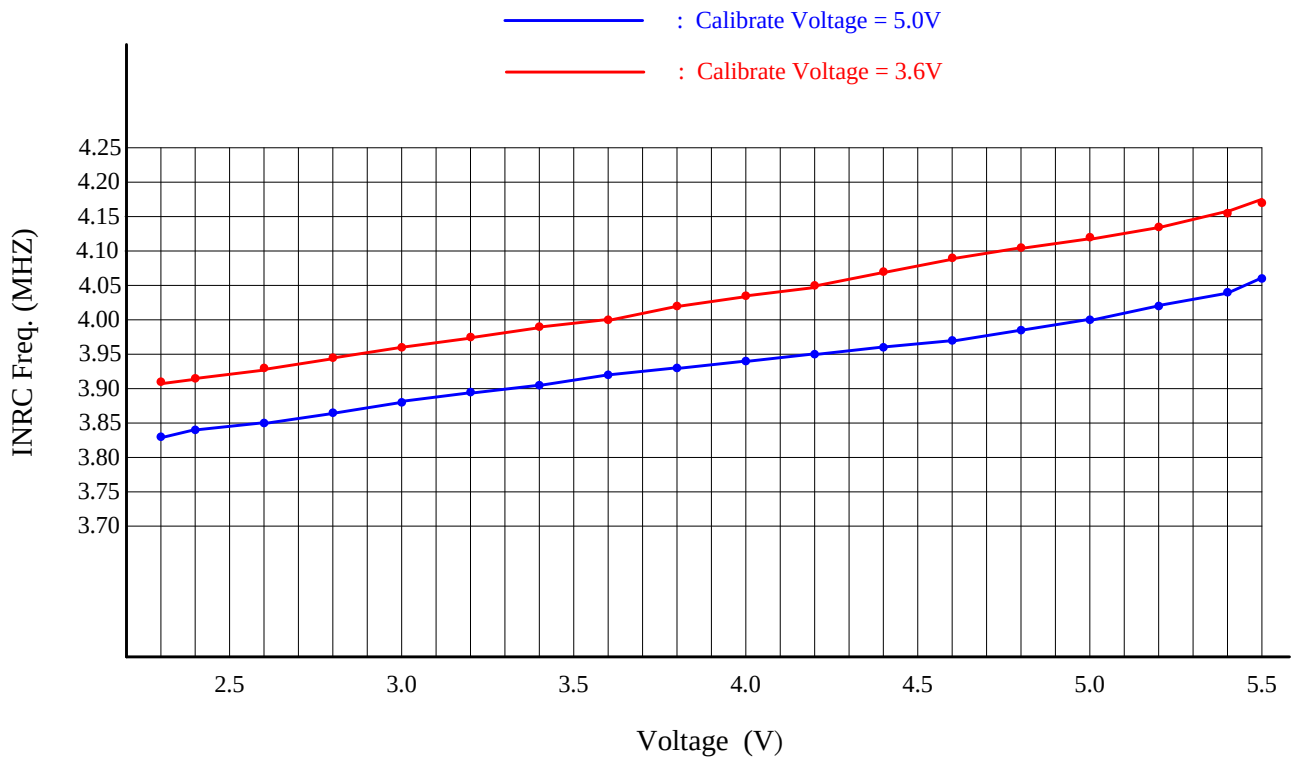
Testing Tempeature Range = -40℃ ~ 125℃



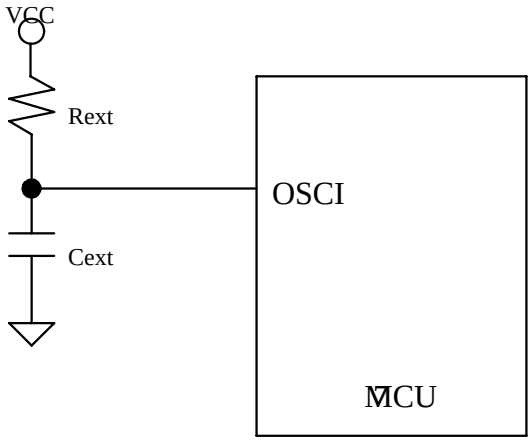
7.5 Internal 4MHZ RC Voltage Characteristic

Power Voltage (VDD) = 2.3V ~ 5V

Typical Temperature = 25℃



7.6 EXT_RC Oscillator Frequencies



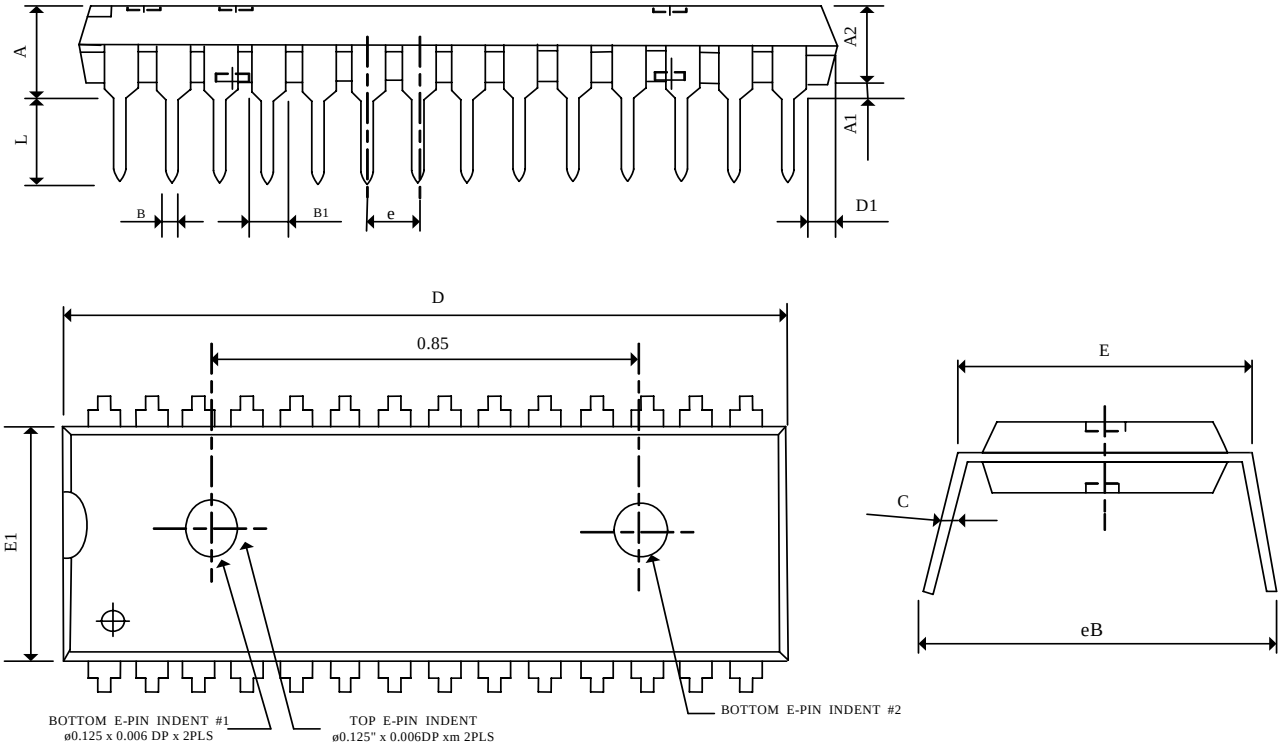
The typical external RC oscillation frequency is as below table

When Cext = 0.01uf (103)

Rext	5V	3V
215K	500 KHZ	435 KHZ
105K	1.0 MHZ	0.95 MHZ
55K	2.0 MHZ	1.9 MHZ
30K	4.0 MHZ	3.95 MHZ
16K	8.0 MHZ	7.7 MHZ
14K	10.0 MHZ	9.0 MHZ

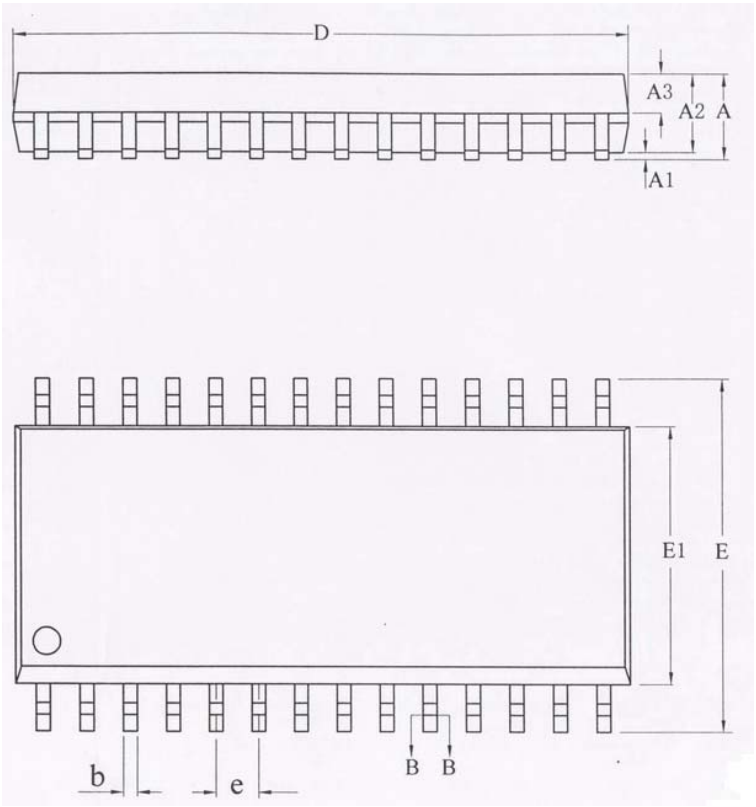
8. Package Dimension

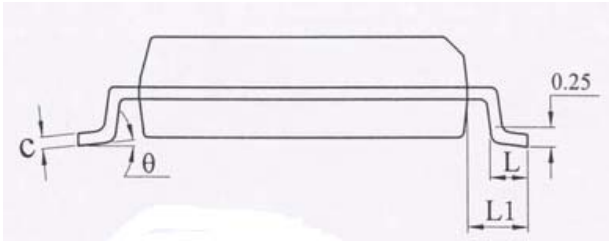
(a) 28 Pin DIP (600 mil)

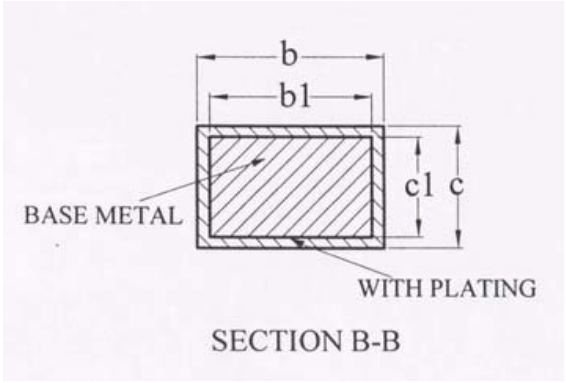


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	5.59	—	—	0.220
A1	0.38	—	—	0.015	—	—
A2	3.71	3.91	4.11	0.146	0.154	0.162
B	0.36	0.46	0.56	0.014	0.018	0.022
B1	1.02	1.27	1.56	0.040	0.050	0.065
C	0.20	0.25	0.33	0.008	0.010	0.013
D	36.58	37.14	37.34	1.440	1.462	1.470
D1	0.13	—	—	0.005	—	—
E	15.24	—	15.88	0.600	—	0.625
E1	13.64	1.89	14.15	0.537	0.547	0.557
e	—	2.54	—	—	0.100	—
L	3.18	—	4.06	0.125	—	0.160
eB	15.88	—	16.89	0.625	—	0.665

(b) 28 Pin SOP

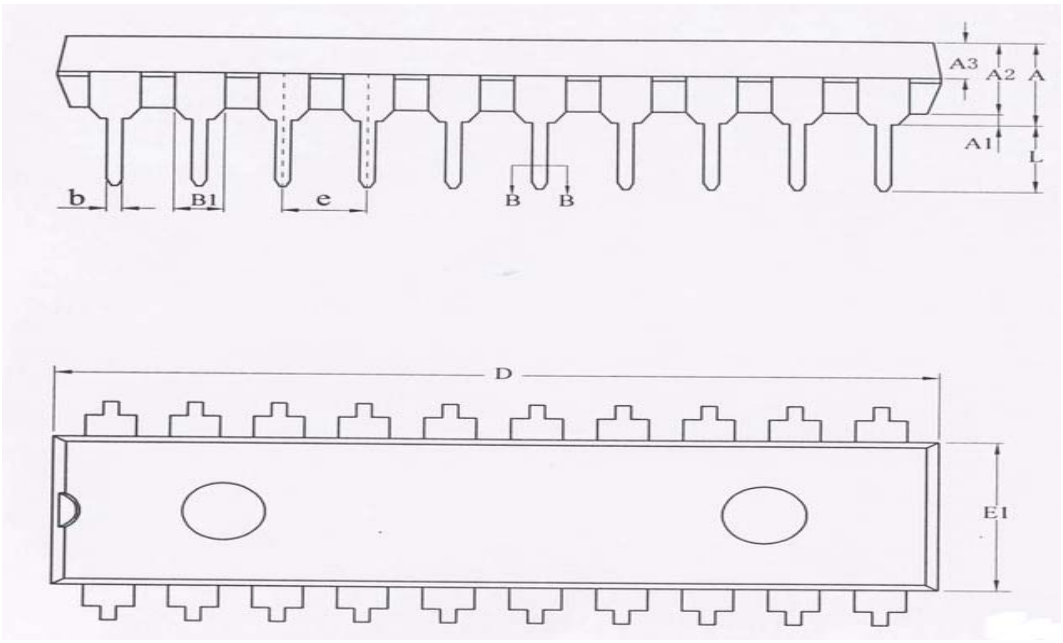


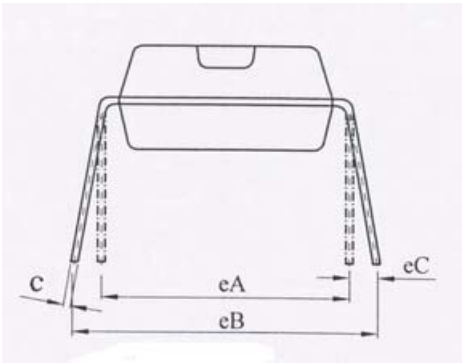


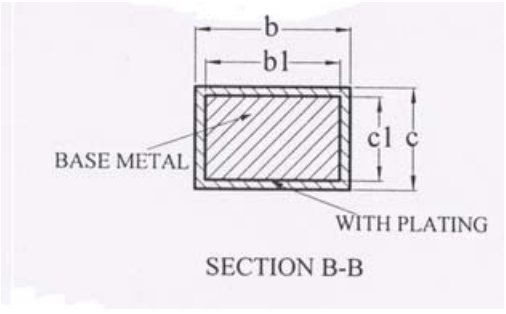


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	2.70
A1	0.10	0.20	0.30
A2	2.10	2.30	2.50
A3	0.92	1.02	1.12
b	0.39	—	0.48
b1	0.38	0.41	0.43
c	0.25	—	0.31
c1	0.24	0.25	0.26
D	17.89	18.09	18.29
E	10.10	10.30	10.50
E1	7.30	7.50	7.70
e	1.27BSC		
L	0.70	0.85	1.00
L1	1.40BSC		
θ	0	—	8°

(c) 20 Pin DIP

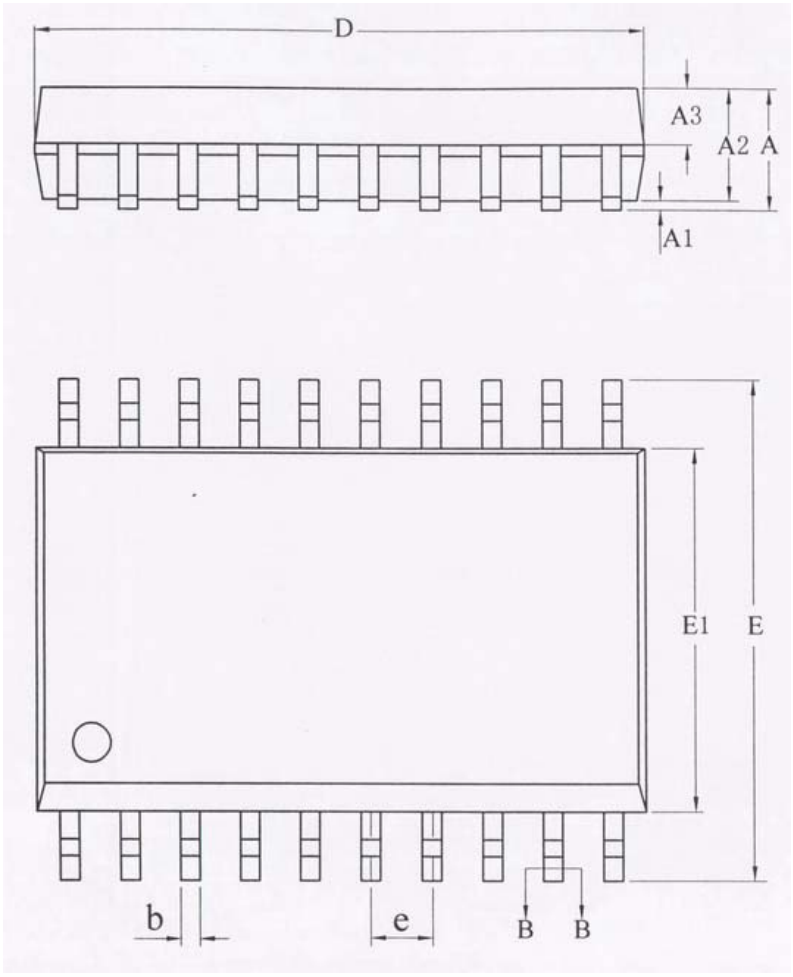






SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	3.60	3.80	4.00
A1	0.51	—	—
A2	3.20	3.30	3.50
A3	1.42	1.52	1.62
b	0.44	—	0.53
b1	0.43	0.46	0.48
B1	1.52BSC		
c	0.25	—	0.31
c1	0.24	0.25	0.26
D	26.03	26.23	26.43
E1	6.35	6.55	6.75
e	2.54BSC		
eA	7.62BSC		
eB	7.62	—	9.50
eC	0	—	0.94
L	3.00	—	—

(d) 20 Pin SOP



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	2.70
A1	0.10	0.20	0.30
A2	2.10	2.30	2.50
A3	0.92	1.02	1.12
b	0.35	—	0.44
b1	0.34	0.37	0.39
c	0.26	—	0.31
c1	0.24	0.25	0.26
D	12.60	12.80	13.00
E	10.10	10.30	10.50
E1	7.30	7.50	7.70
e	1.27BSC		
L	0.70	0.85	1.00
L1	1.40BSC		
θ	0	—	8°