



1. Feature

- ROM size: 2,048 Words OTP ROM
- RAM size: 72 Bytes
- 76 single word instruction
- Stack level: 2
- I/O ports: 20
 - Port B: 8 pull high I/O pin and has wake up function
 - Port A0~3: 4 normal I/O pin
 - Port C0~7: 8 normal I/O pin
 - RTCC: input pin
- Four kinds of external oscillation modes can be selected:
RC, LS(Low Speed) Crystal, NS(Normal Speed) Crystal and HS(High Speed) Crystal
- Port B has signal toggle wake up function
- Built-in one 8 bit count up Timer/counter (TMR0) with 8 bit programmable prescaler
- Built-in Watchdog Timer
- Operation Voltage: 2.2V 5.5V
- Different Package Type:
 - MK7A20PD28C: 28 pin DIP
 - MK7A20PSD28C: 28 pin SDIP
 - MK7A20PS28C: 28 pin SOP
 - MK7A20PSS28C: 28 pin SSOP
 - MK7A20PSD20C: 20 pin SDIP
 - MK7A20PS20C: 20 pin SOP
 - MK7A20PSD18C: 18 pin SDIP
 - MK7A20PS18C: 18 pin SOP



2. Pin Assignment

| | | | | |
|------|----|---|----|--------|
| RTCC | 1 | ● | 28 | RESETB |
| VDD | 2 | | 27 | OSC1 |
| NC | 3 | | 26 | OSC2 |
| VSS | 4 | | 25 | PC7 |
| NC | 5 | | 24 | PC6 |
| PA0 | 6 | | 23 | PC5 |
| PA1 | 7 | | 22 | PC4 |
| PA2 | 8 | | 21 | PC3 |
| PA3 | 9 | | 20 | PC2 |
| PB0 | 10 | | 19 | PC1 |
| PB1 | 11 | | 18 | PC0 |
| PB2 | 12 | | 17 | PB7 |
| PB3 | 13 | | 16 | PB6 |
| PB4 | 14 | | 15 | PB5 |

28 pin SDIP, DIP or SOP package

| | | | | |
|------|----|---|----|--------|
| VSS | 1 | ● | 28 | RESETB |
| RTCC | 2 | | 27 | OSC1 |
| VDD | 3 | | 26 | OSC2 |
| VDD | 4 | | 25 | PC7 |
| PA0 | 5 | | 24 | PC6 |
| PA1 | 6 | | 23 | PC5 |
| PA2 | 7 | | 22 | PC4 |
| PA3 | 8 | | 21 | PC3 |
| PB0 | 9 | | 20 | PC2 |
| PB1 | 10 | | 19 | PC1 |
| PB2 | 11 | | 18 | PC0 |
| PB3 | 12 | | 17 | PB7 |
| PB4 | 13 | | 16 | PB6 |
| VSS | 14 | | 15 | PB5 |

28 pin SSOP package

| | | | | |
|--------|----|---|----|-----|
| PC4 | 1 | ● | 20 | PC3 |
| PC5 | 2 | | 19 | PB7 |
| PC6 | 3 | | 18 | PB6 |
| PC7 | 4 | | 17 | PB5 |
| OSC2 | 5 | | 16 | PB4 |
| OSC1 | 6 | | 15 | PB3 |
| RESETB | 7 | | 14 | PB2 |
| VDD | 8 | | 13 | PB1 |
| VSS | 9 | | 12 | PB0 |
| PA0 | 10 | | 11 | PA1 |

20 pin SDIP and SOP package

| | | | | |
|--------|---|---|----|-----|
| PC5 | 1 | ● | 18 | PB7 |
| PC6 | 2 | | 17 | PB6 |
| PC7 | 3 | | 16 | PB5 |
| OSC2 | 4 | | 15 | PB4 |
| OSC1 | 5 | | 14 | PB3 |
| RESETB | 6 | | 13 | PB2 |
| VDD | 7 | | 12 | PB1 |
| VSS | 8 | | 11 | PB0 |
| PA0 | 9 | | 10 | PA1 |

18 pin SDIP and SOP package

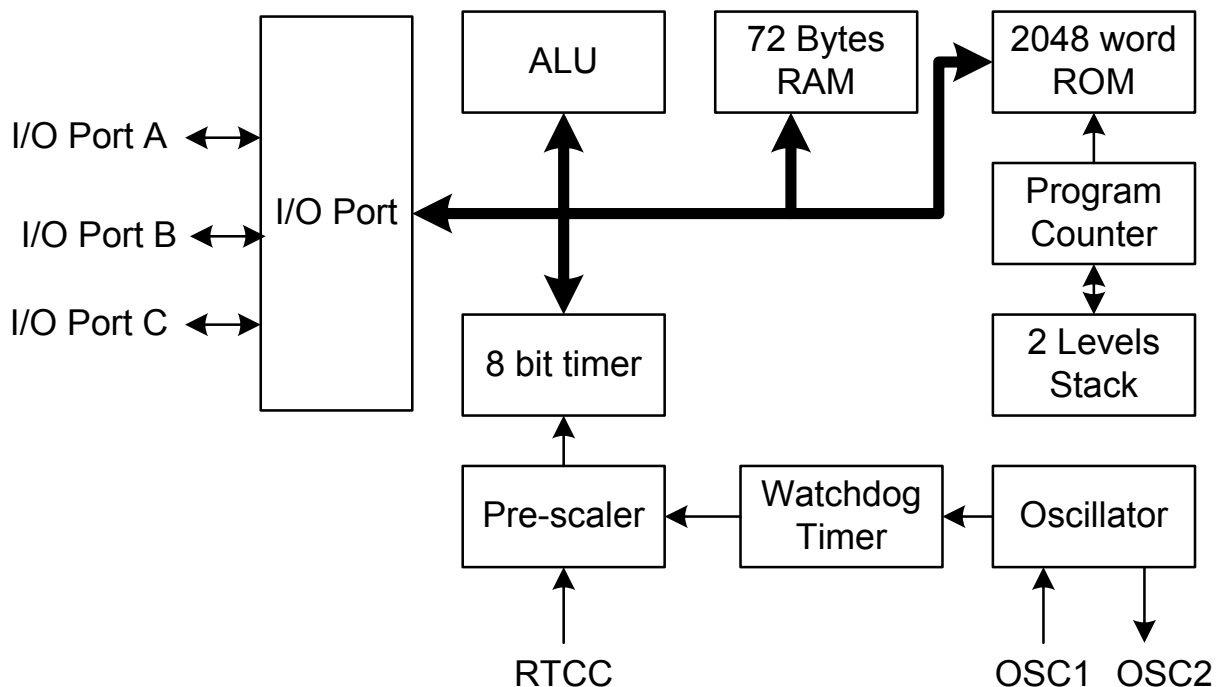


3. Pin Description

| Name | I/O | Description |
|--------|-----|---|
| RTCC | I | 1. External clock or pulse input to TMR0 counter 2. PA4 input (When config bit6 is set to1) |
| PA3~0 | I/O | I/O Port A0~3 |
| PB7~0 | I/O | 1. I/O Port B0~7 2. Signal toggle wake up (When config bit7 is set to1) 3. Pull-up resistor (When config bit7 is set to1) |
| PC7~0 | I/O | I/O Port C0~7 |
| RESETB | I | System reset signal |
| OSC1 | I | Oscillator input |
| OSC2 | O | Oscillator output |
| VDD | P | System power |
| VSS | P | Ground |

<Note> I: Input; O: Output; I/O: Input/Output; P: Power

4. System Block Diagram





5. Memory Map

5.1 Program memory

| | |
|---------------------|--------|
| 000H | PAGE 0 |
| 1FFH | |
| 200H | PAGE 1 |
| 3FFH | |
| 400H | PAGE 2 |
| 5FFH | |
| 600H | PAGE 3 |
| 7FFH (RESET VECTOR) | |

<Note> LCALL and LGOTO allow directly operate 2K word addressing.

5.2 Control Register

| Name | Addr | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------|------|-------|-------|-------|-------|-------|-------|-------|-------|
| CONFIG | | TYPE | RTCE | LV1 | LV0 | CPT | WDTE | FOSC1 | FOSC0 |
| SELECT | | X | X | SUR0 | EDGE0 | PSA | PS2 | PS1 | PS0 |
| IAR | \$00 | X | X | X | A4 | A3 | A2 | A1 | A0 |
| TMR0 | \$01 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| PC | \$02 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| STATUS | \$03 | X | SA1 | SA0 | TOB | PDB | Z | DC | C |
| BSR | \$04 | X | X | X | D4 | D3 | D2 | D1 | D0 |
| I/O Port A | \$05 | X | X | X | X | PA3 | PA2 | PA1 | PA0 |
| I/O Port B | \$06 | PB7 | PB6 | PB5 | PB4 | PB3 | PB2 | PB1 | PB0 |
| I/O Port C | \$07 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |



5.3 Configuration Register

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| CONFIG | TYPE | RTCE | LV1 | LV0 | CPT | WDTE | FOSC1 | FOSC0 |

| Bit 1 | Bit 0 | OSC Type | Frequency Range |
|-------|-------|-------------------|-----------------|
| 0 | 0 | LS (low speed) | 32~200KHz |
| 0 | 1 | NS (Normal speed) | 200K~10MHz |
| 1 | 0 | HS (high speed) | 10~20MHz |
| 1 | 1 | RC | 32K~ 10MHz |

| Bit 2 | Description |
|-------|------------------------|
| 0 | Watchdog timer disable |
| 1 | Watchdog timer enable |

| Bit 3 | Description |
|-------|---------------------|
| 0 | Code Protection ON |
| 1 | Code Protection OFF |

| Bit 5 | Bit 4 | Detected Voltage Level |
|-------|-------|------------------------|
| 0 | 0 | 4V |
| 0 | 1 | No use |
| 1 | 0 | 2V |
| 1 | 1 | No use |

| Bit 6 | Description |
|-------|------------------|
| 0 | Timer Input Only |
| 1 | PA4 Input |



| Bit 7 | Description |
|-------|--|
| 0 | Port B has no signal toggle wake up function |
| 1 | Port B has signal toggle wake up function |

<Note> When Port B is in input mode, it will has pull up resistor

5.4 Select Register

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|
| SELECT | | | SUR0 | EDGE0 | PSA | PS2 | PS1 | PS0 |

| Bit 2 | Bit 1 | Bit 0 | Description | |
|-------|-------|-------|-------------|----------|
| PS2 | PS1 | PS0 | TMR0 rate | WDT rate |
| 0 | 0 | 0 | 1:2 | 1:1 |
| 0 | 0 | 1 | 1:4 | 1:2 |
| 0 | 1 | 0 | 1:8 | 1:4 |
| 0 | 1 | 1 | 1:16 | 1:8 |
| 1 | 0 | 0 | 1:32 | 1:16 |
| 1 | 0 | 1 | 1:64 | 1:32 |
| 1 | 1 | 0 | 1:128 | 1:64 |
| 1 | 1 | 1 | 1:256 | 1:128 |

| Bit 3 | Description |
|-------|----------------------------|
| 0 | Prescaler assigned to TMR0 |
| 1 | Prescaler assigned to WDT |

| Bit 4 | Description |
|-------|---|
| 0 | Increment when rising edge (Lo to Hi transition) on external clock |
| 1 | Increment when falling edge (Hi to Lo transition) on external clock |

| Bit 5 | Description |
|-------|---------------------------------------|
| 0 | TMR0 clock source is (System Clock/4) |
| 1 | TMR0 clock source is RTCC input |



5.5 Data memory (Register and RAM)

The Data memory is composed of Register and RAM, the address map is as below:

| | BANK0 | BANK1 | BANK2 | BANK3 |
|-----|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|
| 00H | IAR | | | |
| 01H | TMR0 | | | |
| 02H | PC | | | |
| 03H | STATUS | | | |
| 04H | BSR | | | |
| 05H | PORT A | | | |
| 06H | PORT B | | | |
| 07H | PORT C | | | |
| 08H | General Purpose Register | | | |
| 0FH | General Purpose Register | | | |
| | General Purpose Registers 10H~1FH | General Purpose Registers 30H~3FH | General Purpose Registers 50H~5FH | General Purpose Registers 70H~7FH |

5.5.1 IAR: Indirect Address Register. It is used with BSR to access a physical address.

5.5.2 TMR0: 8 bit count up timer register.

5.5.3 PC: Program Counter. 11 bit counter register.



5.5.4 STATUS: Status Register.

| Bit | Symbol | Description | | |
|-----|---------|---|---|--------------------|
| 0 | C | Carry and Borrow bit: | | |
| | | ADD instruction | SUB instruction | |
| | | 1: a carry occurred from the MSB 0: no carry | 1: no borrow ^(Note1) 0: a borrow occurred from the MSB | |
| 1 | DC | Nibble Carry and Nibble Borrow bit | | |
| | | ADD instruction | SUB instruction | |
| | | 1: a carry from the low nibble bits of the result occurred 0: no carry | 1: no borrow 0: a borrow from the low nibble bits of the result occurred | |
| 2 | Z | Zero bit: 1: the result of a logic operation is zero 0: the result of a logic operation is not zero | | |
| 3 | PDB | Power down flag bit: ^(Note2) 1: after power-on or by the CLRWDT instruction 0: execute SLEEP instruction | | |
| 4 | TOB | Time out flag bit: 1: after power-on or by the CLRWDT or SLEEP instruction 0: Occur WDT time-overflow | | |
| 6~5 | SA1~SA0 | SA1 | SA0 | Page Location |
| | | 0 | 0 | Page 0 (000H~1FFH) |
| | | 0 | 1 | Page 1 (200H~3FFH) |
| | | 1 | 0 | Page 2 (400H~5FFH) |
| | | 1 | 1 | Page 3 (600H~7FFH) |

<Note1>: A SUB instruction is executed by adding the 2's complement of the subtrahend, so C = 1 represents positive result. The below table show the relation between Carry and Borrow.

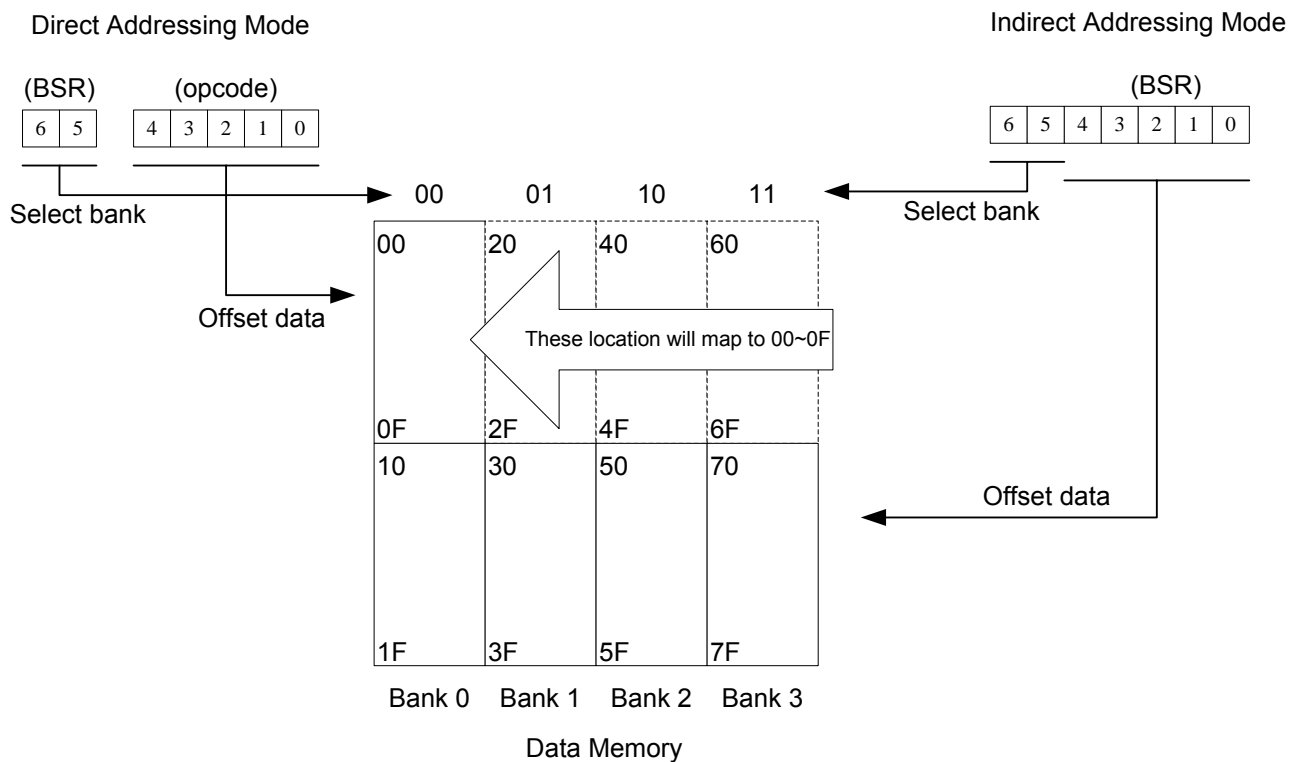
| B0H - 50H | | | | | | | | | | 50H - B0H | | | | | | | | | |
|-----------|---|----|----|----|----|----|----|----|----|-----------|---|----|----|----|----|----|----|----|----|
| | C | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | | C | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| + | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | + | | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| = | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | = | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |



<Note2>: The TOB and PDB bits are active low that can be used to determine different causes of reset. The below table illustrates the value of TOB and PDB after the relative reset events.

| TOB | PDB | Reset Event |
|-----------|-----------|-------------------------------|
| 0 | 0 | WDT time out from sleep mode |
| 0 | 1 | WDT time out from normal mode |
| 1 | 0 | RESETB reset from sleep |
| 1 | 1 | Power on reset |
| Unchanged | Unchanged | RESETB reset from normal |

5.5.5 BSR: Bank Select Register. It is used with IAR for indirect addressing data memory.



5.5.6 Port A/B/C are programmable I/O ports. All I/O pins were set to input mode in power on reset stage.



5.6 Reset

There are 4 kinds of condition will cause system reset:

5.6.1 Power-on

5.6.2 LVR (low power reset)

5.6.3 Input a Lo signal into RESETB

5.6.4 When WDTE flag is enabled and the timer escape

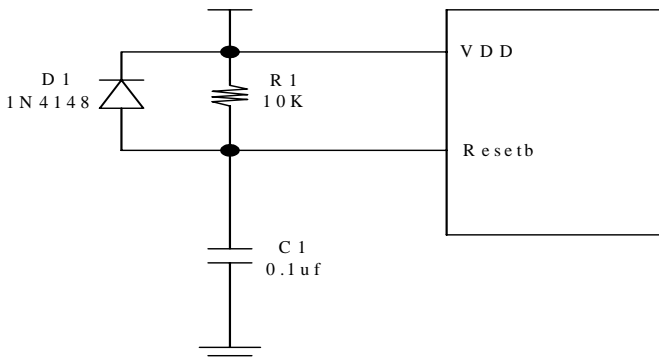


Fig.5.6.1 RESETB PIN circuit

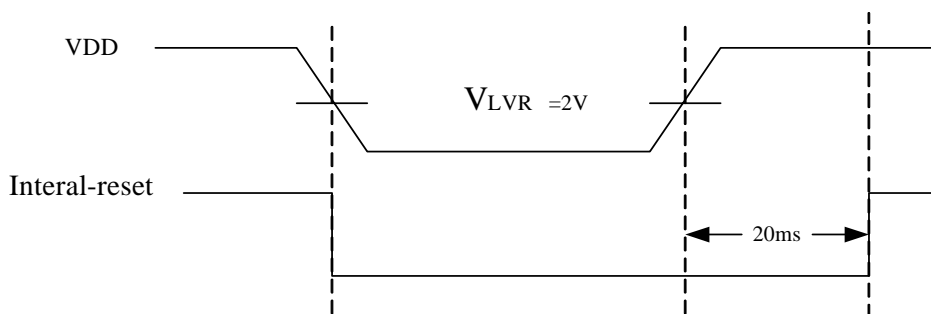


Fig.5.6.2 LVR ON & VDD voltage

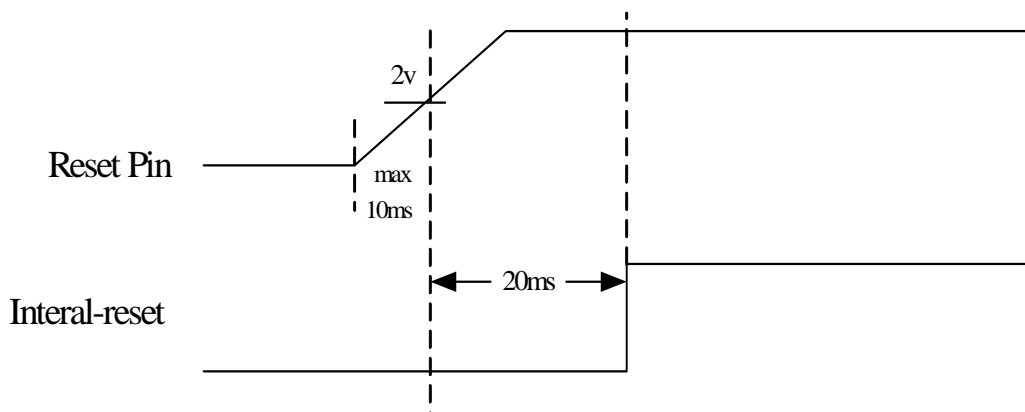


Fig.5.6.3 LVR OFF , RESETB & VDD voltage timing



5.7 Reset condition of all the RAM

| Address | Name | Cold Reset | Warm Reset |
|---------|---------------------|---------------|---------------|
| N/A | Accumulator | xxxx xxxx | pppp pppp |
| N/A | IODIR | 1111 1111 | 1111 1111 |
| N/A | Select | --11 1111 | --11 1111 |
| 00h | IAR | ---- ---- | ---- ---- |
| 01h | TMR0 | xxxx xxxx | pppp pppp |
| 02h | PC | 111 1111 1111 | 111 1111 1111 |
| 03h | STATUS | 0001 1xxx | 000# #ppp |
| 04h | BSR | 1xxx xxxx | 1ppp pppp |
| 05h | PORTA | 0000 xxxx | 0000 pppp |
| 06h | PORTB | xxxx xxxx | pppp pppp |
| 07h | PORTC | xxxx xxxx | pppp pppp |
| | General Purpose RAM | xxxx xxxx | pppp pppp |

<Note> x: unknown; p: keep as previous data ; #: value depends on condition
-:unimplemented and read as"0".



5.8 Wake up function

The chip provide pin signal toggle wake up function. It will return from sleep mode when signal toggle in input port. In order to safely wake up from sleep mode, we suggest to read the input pin to store data before entering sleep mode. The sample program is as below:

```
MOVLA    FFh
IODIR    PORTB  ;// set bit0~7 of port B as input. Only input pin can be wake up
.....
MOV      PORTB,a ;//Store the data of input pin before sleep
SLEEP                                ;// if doesn't perform the read instruction, then can not enter
                                        ;// SLEEP mode
NOP                                       ;//Add NOP instruction to delay a while when chi
```



6. Instruction Set

<Note> Instruction cycle consist of 4 system clock

| Mnemonic Operands | Instruction Code (Advance) | Cycles | Status Affected | OP-code |
|-------------------|---|------------|-----------------|---------------------|
| ADD M, m | (M)+(acc) (M) | 1 | C, DC, Z | 01 0101 1MMM MMMM |
| ADD M, a | (M)+(acc) (acc) | 1 | C, DC, Z | 01 0101 0MMM MMMM |
| AND M, m | (M) . (acc) (M) | 1 | Z | 01 0100 1MMM MMMM |
| AND M, a | (M) . (acc) (acc) | 1 | Z | 01 0100 0MMM MMMM |
| ANDLA I | Literal . (acc) (acc) | 1 | Z | 11 1001 iiiii iiiii |
| BC M, b0 | Clear bit0 of (M) | 1 | None | 00 1100 0MMM MMMM |
| BC M, b1 | Clear bit1 of (M) | 1 | None | 00 1100 1MMM MMMM |
| BC M, b2 | Clear bit2 of (M) | 1 | None | 00 1101 0MMM MMMM |
| BC M, b3 | Clear bit3 of (M) | 1 | None | 00 1101 1MMM MMMM |
| BC M, b4 | Clear bit4 of (M) | 1 | None | 00 1110 0MMM MMMM |
| BC M, b5 | Clear bit5 of (M) | 1 | None | 00 1110 1MMM MMMM |
| BC M, b6 | Clear bit6 of (M) | 1 | None | 00 1111 0MMM MMMM |
| BC M, b7 | Clear bit7 of (M) | 1 | None | 00 1111 1MMM MMMM |
| BS M, b0 | Set bit0 of (M) | 1 | None | 00 1000 0MMM MMMM |
| BS M, b1 | Set bit1 of (M) | 1 | None | 00 1000 1MMM MMMM |
| BS M, b2 | Set bit2 of (M) | 1 | None | 00 1001 0MMM MMMM |
| BS M, b3 | Set bit3 of (M) | 1 | None | 00 1001 1MMM MMMM |
| BS M, b4 | Set bit4 of (M) | 1 | None | 00 1010 0MMM MMMM |
| BS M, b5 | Set bit5 of (M) | 1 | None | 00 1010 1MMM MMMM |
| BS M, b6 | Set bit6 of (M) | 1 | None | 00 1011 0MMM MMMM |
| BS M, b7 | Set bit7 of (M) | 1 | None | 00 1011 1MMM MMMM |
| BTSC M, b0 | If bit0 of (M) = 0, skip next instruction | 1 + (skip) | None | 00 0100 0MMM MMMM |
| BTSC M, b1 | If bit1 of (M) = 0, skip next instruction | 1 + (skip) | None | 00 0100 1MMM MMMM |
| BTSC M, b2 | If bit2 of (M) = 0, skip next instruction | 1 + (skip) | None | 00 0101 0MMM MMMM |
| BTSC M, b3 | If bit3 of (M) = 0, skip next instruction | 1 + (skip) | None | 00 0101 1MMM MMMM |
| BTSC M, b4 | If bit4 of (M) = 0, skip next instruction | 1 + (skip) | None | 00 0110 0MMM MMMM |
| BTSC M, b5 | If bit5 of (M) = 0, skip next instruction | 1 + (skip) | None | 00 0110 1MMM MMMM |
| BTSC M, b6 | If bit6 of (M) = 0, skip next instruction | 1 + (skip) | None | 00 0111 0MMM MMMM |



| | | | | |
|------------|---|------------|--------|-------------------|
| BTSC M, b7 | If bit7 of (M) = 0, skip next instruction | 1 + (skip) | None | 00 0111 1MMM MMMM |
| BTSS M, b0 | If bit0 of (M) = 1, skip next instruction | 1 + (skip) | None | 00 0000 0MMM MMMM |
| BTSS M, b1 | If bit1 of (M) = 1, skip next instruction | 1 + (skip) | None | 00 0000 1MMM MMMM |
| BTSS M, b2 | If bit2 of (M) = 1, skip next instruction | 1 + (skip) | None | 00 0001 0MMM MMMM |
| BTSS M, b3 | If bit3 of (M) = 1, skip next instruction | 1 + (skip) | None | 00 0001 1MMM MMMM |
| BTSS M, b4 | If bit4 of (M) = 1, skip next instruction | 1 + (skip) | None | 00 0010 0MMM MMMM |
| BTSS M, b5 | If bit5 of (M) = 1, skip next instruction | 1 + (skip) | None | 00 0010 1MMM MMMM |
| BTSS M, b6 | If bit6 of (M) = 1, skip next instruction | 1 + (skip) | None | 00 0011 0MMM MMMM |
| BTSS M, b7 | If bit7 of (M) = 1, skip next instruction | 1 + (skip) | None | 00 0011 1MMM MMMM |
| CLRA | Clear accumulator | 1 | Z | 01 0001 0000 0000 |
| CLR M | Clear memory M | 1 | Z | 01 0001 1MMM MMMM |
| CLRWDT | Clear watch-dog register | 1 | TO, PO | 01 0000 0000 0001 |
| COM M, m | ~(M) (M) | 1 | Z | 01 0010 1MMM MMMM |
| COM M, a | ~(M) (acc) | 1 | Z | 01 0010 0MMM MMMM |
| DEC M, m | Decrement M to M | 1 | Z | 01 0110 1MMM MMMM |
| DEC M, a | (M) - 1 (acc) | 1 | Z | 01 0110 0MMM MMMM |
| DECSZ M, m | (M) - 1 (M), skip if (M) = 0 | 1 + (skip) | None | 01 0111 1MMM MMMM |
| DECSZ M, a | (M) - 1 (acc), skip if (M) = 0 | 1 + (skip) | None | 01 0111 0MMM MMMM |
| INC M, m | (M) + 1 (M) | 1 | Z | 01 1000 1MMM MMMM |
| INC M, a | (M) + 1 (acc) | 1 | Z | 01 1000 0MMM MMMM |
| INCSZ M, m | (M) + 1 (M), skip if (M) = 0 | 1 + (skip) | None | 01 1001 1MMM MMMM |
| INCSZ M, a | (M) + 1 (acc), skip if (M) = 0 | 1 + (skip) | None | 01 1001 0MMM MMMM |
| IODIR M | Set i/o direction | 1 | None | 01 0000 0000 0MMM |
| IOR M, m | (M) ior (acc) (M) | 1 | Z | 01 1111 1MMM MMMM |
| IOR M, a | (M) ior (acc) (acc) | 1 | Z | 01 1111 0MMM MMMM |
| IORLA I | Literal ior (acc) (acc) | 1 | Z | 11 0011 iiiiiiii |
| LCALL I | Call subroutine. However, LCALL can addressing 2K address | 2 | None | 10 0iii iiiiiiii |
| LGOTO I | Go branch to any address | 2 | None | 10 1iii iiiiiiii |



| | | | | |
|-----------|--|---|----------|-------------------|
| MOVAM m | Move data form acc to memory | 1 | None | 01 0000 1MMM MMMM |
| MOVLA I | Move literal to accumulator | 1 | None | 11 0001 iiiiiiii |
| MOV M, m | (M) (M) | 1 | Z | 01 0011 1MMM MMMM |
| MOV M, a | (M) (acc) | 1 | Z | 01 0011 0MMM MMMM |
| NOP | No operation | 1 | None | 01 0000 0000 0000 |
| RET | Return | 2 | None | 11 1111 0111 1111 |
| RETI | Return and enable INTM | 2 | None | 11 1111 1111 1111 |
| RETLA I | Return and move literal to accumulator | 2 | None | 11 1100 iiiiiiii |
| RL M, m | Rotate left from m to itself | 1 | C | 01 1100 1MMM MMMM |
| RL M, a | Rotate left from m to acc | 1 | C | 01 1100 0MMM MMMM |
| RR M, m | Rotate right from m to itself | 1 | C | 01 1110 1MMM MMMM |
| RR M, a | Rotate right from m to acc | 1 | C | 01 1110 0MMM MMMM |
| SELECT | Set select register | 1 | None | 01 0000 0000 0010 |
| SLEEP | Enter sleep (saving) mode | 1 | TO, PO | 01 0000 0000 0011 |
| SUB M, m | (M)-(acc) (M) | 1 | C, DC, Z | 01 1010 1MMM MMMM |
| SUB M, a | (M)-(acc) (acc) | 1 | C, DC, Z | 01 1010 0MMM MMMM |
| SWAP M, m | Swap data from m to itself | 1 | None | 01 1101 1MMM MMMM |
| SWAP M, a | Swap data from m to acc | 1 | None | 01 1101 0MMM MMMM |
| XOR M, m | (M) xor (acc) (M) | 1 | Z | 01 1011 1MMM MMMM |
| XOR M, a | (M) xor (acc) (acc) | 1 | Z | 01 1011 0MMM MMMM |
| XORLA I | Literal xor (acc) (acc) | 1 | Z | 11 1000 iiiiiiii |



7. Electrical Characteristics

7.1 Absolute Maximum Ratings

Supply Voltage Vss-0.3V to Vss+5.5V Storage Temperature -50 to 125
Input Voltage Vss-0.3V to VDD+0.3V Operating Temperature 0 to 70

7.2 DC Characteristics

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|-------------------|-----------------------|-----------------|--|------|------|------|------|
| | | VDD | Conditions | | | | |
| VDD | Operating Voltage | --- | | 2.2 | | 5.5 | V |
| V _{DVT} | Detect Voltage | 5V | Low Voltage Detector (I _{dd} = 3uA) Config bit6.bit5=00 | | 3.8 | | V |
| | | 3V | Low Voltage Detector (I _{dd} = 1uA) Config bit6.bit5=10 | | 2.2 | | V |
| V _{IL} | Input Low Voltage | 5V | I/O Port | | | 0.8 | V |
| I _{DD1} | Standby Current | 5V | WDT disable | | 1 | | UA |
| | | | WDT enable | | 10 | | |
| I _{IL} | Input Leakage Current | 5V | Vin=VDD, VSS | | 1 | | UA |
| I _{DD1} | Standby Current | 5V | LVD disable,WDT disable, LV disable | | 1 | | |
| | | | LVD disable,WDT enable, LV disable | | 10 | | |
| | | 3V | LVD disable,WDT disable, LV disable | | 1 | | |
| | | | LVD disable,WDT enable, LV disable | | 2 | | |
| I _{IL} | Input Leakage Current | 5V | Vin=VDD, VSS | | 1 | | uA |
| | | | Vol=01V | | 35 | | |
| | | | Vol=1.5V | | 50 | | |
| R _{PUHI} | Pull_Hi Pin Resistor | 5V | Set PortB input pin and Pull_Hi | | 60 | | KΩ |
| | | 3V | Set PortB input pin and Pull_Hi | | 100 | | |



| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|----------|---|-----------------|------------|------|------|------|------|
| | | VDD | Conditions | | | | |
| I_{OH} | PA0~3 output port , PB0~7 output port, PC0~3 output port, Driving Current | 5V | Voh=4.5V | | 9 | | mA |
| | | | Voh=4.0V | | 18 | | mA |
| | | | Voh=3.5V | | 22 | | mA |
| | | | Voh=3.0V | | 26 | | mA |
| | | | Voh=2.5V | | 29 | | mA |
| | | 3V | Voh=2.7V | | 4 | | mA |
| | | | Voh=2.4V | | 7 | | mA |
| | | | Voh=2.1V | | 9 | | mA |
| | | | Voh=2.1V | | 10 | | mA |
| | | | Voh=1.8V | | 12 | | mA |
| I_{OL} | PA0~3 output port , PB0~7 output port, PC0~3 output port, Sink Current | 5V | Voh=0.5V | | 20 | | mA |
| | | | Voh=1.0V | | 37 | | mA |
| | | | Voh=1.5V | | 48 | | mA |
| | | | Voh=2.0V | | 55 | | mA |
| | | | Voh=2.5V | | 59 | | mA |
| | | 3V | Voh=0.3V | | 8 | | mA |
| | | | Voh=0.6V | | 16 | | mA |
| | | | Voh=0.9V | | 21 | | mA |
| | | | Voh=1.2V | | 25 | | mA |
| | | | Voh=1.5V | | 26 | | mA |



7.3 AC Characteristics

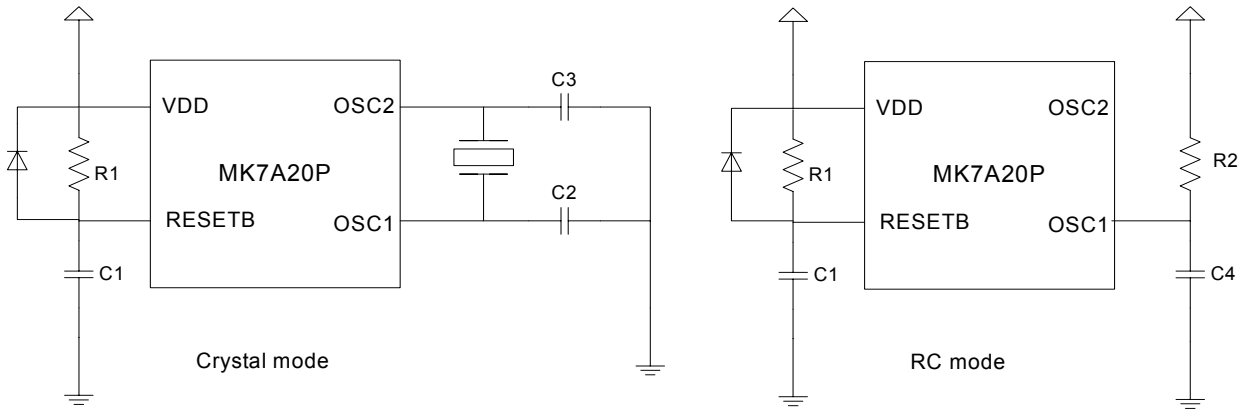
| Symbol | Parameter | Test Conditions | | Min | Typ | Max | Unit |
|-------------------|-----------------|-----------------|-----------------|-----|-----|-----|------|
| | | VDD | Conditions | | | | |
| f _{sys1} | System Clock | 5V | LP Crystal mode | 32 | | 455 | Khz |
| | | 3V | | 32 | | 455 | |
| f _{sys2} | System Clock | 5V | NT Crystal mode | 1 | | 10 | Mhz |
| | | 3V | | 1 | | 10 | |
| f _{sys3} | System Clock | 5V | HS Crystal mode | 10 | | 20 | Mhz |
| | | 3V | | 10 | | 20 | |
| f _{sys4} | System Clock | 5V | RC mode | 32K | | 10 | Mhz |
| | | 3V | | 32K | | 10 | |
| T _{wdt} | Watchdog Timer | 5V | | | 20 | | mS |
| | | 3V | | | 25 | | |
| T _{rht} | Reset Hold Time | 5V | | | 20 | | mS |
| | | 3V | | | 25 | | |

7.4 External RC Table

| R value | C value | RC frequency | R connect to (VDD,OSC1) |
|---------|----------------|--------------|---|
| 4.9 M | 0.1u (need) | 32 Khz | The capacitor is need for stabile frequency |
| 250 K | 0.1u (suggest) | 455 Khz | |
| 116 K | 0.1u (suggest) | 1 Mhz | |
| 60 K | 0.1u (suggest) | 2 Mhz | |
| 32 K | 0.1u (suggest) | 4 Mhz | |
| 18 K | 0.1u (suggest) | 8 Mhz | |
| 14 K | 0.1u (suggest) | 10 Mhz | |



7.5 Oscillator circuit in different mode



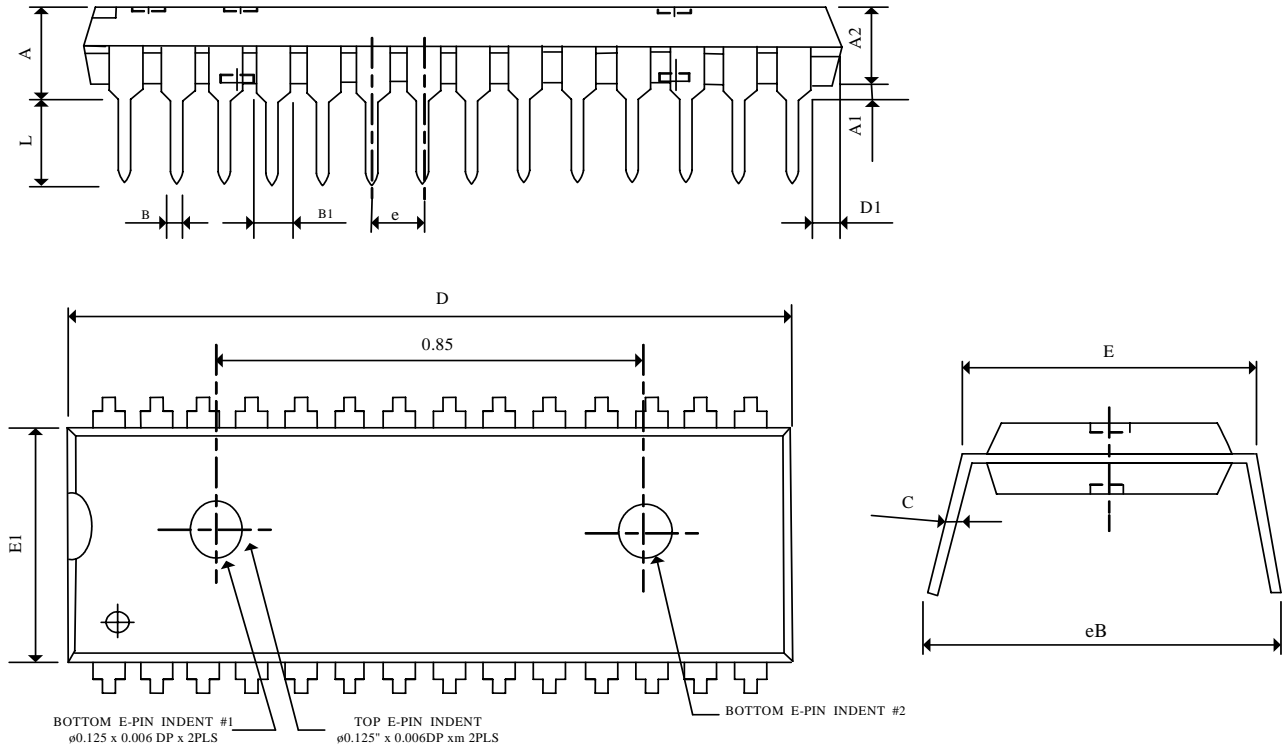
| Crystal mode | Crystal | C2 | C3 |
|--------------|---------|---------|---------|
| LP mode | 32 KHz | 20~100P | 20~100P |
| | 455 KHz | 100P | 100P |
| NT mode | 455 KHz | 100P | 100P |
| | 1 Mhz | 20~100P | 20~100P |
| | 2 Mhz | 20~100P | 20~100P |
| | 4 Mhz | 20~100P | 20~100P |
| | 8 Mhz | 20~50P | 20~50P |
| HS mode | 10 Mhz | 20~50P | 20~50P |
| | 12 Mhz | 20~50P | 20~50P |
| | 16 Mhz | 20~50P | 20~50P |
| | 20 Mhz | 20~50P | 20~50P |

<Note> R1/C1 value of RESETB depends on user's system request



8. Package Dimension

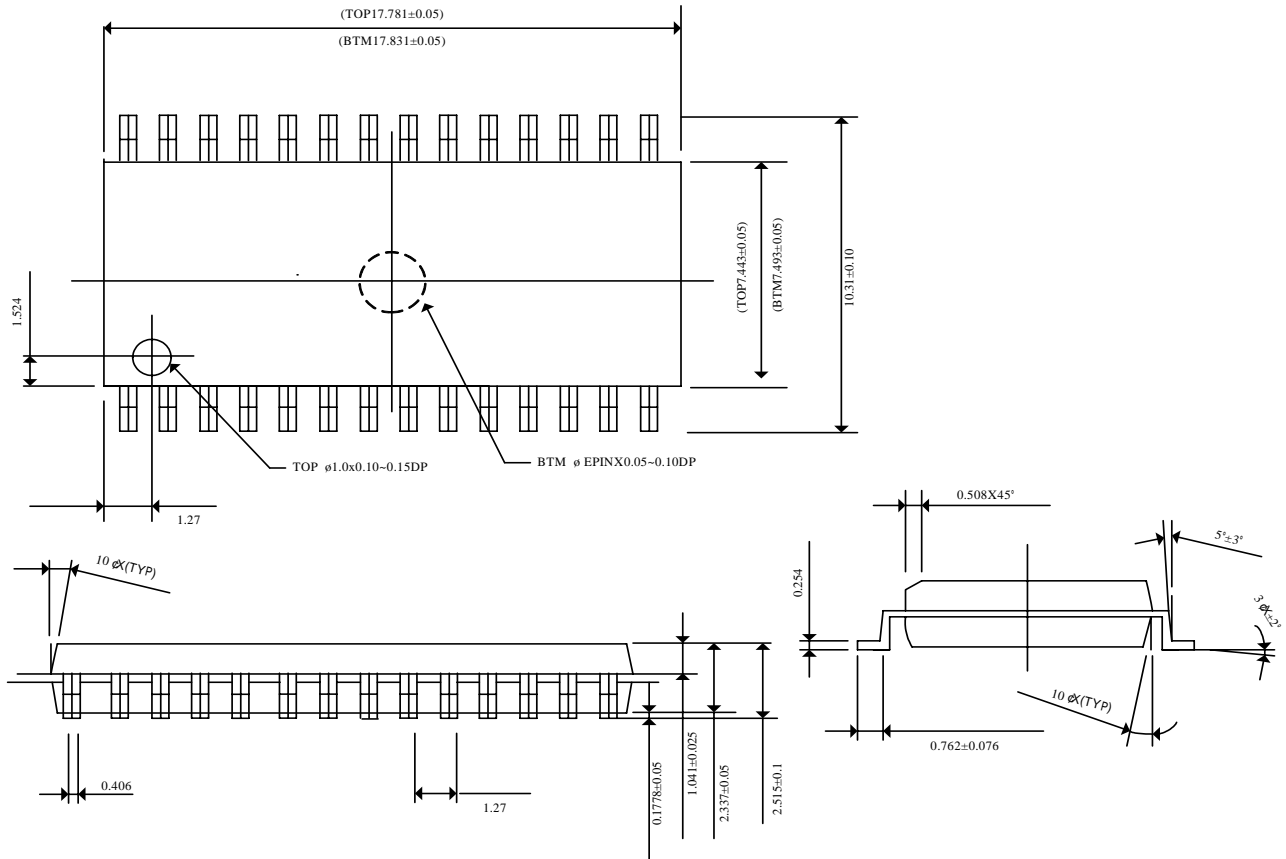
(a) 28 Pin DIP (600 mil)



| SYMBOLS | DIMENSIONS IN MILLIMETERS | | | DIMENSIONS IN INCHES | | |
|---------|---------------------------|-------|-------|----------------------|-------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | | | 5.59 | | | 0.220 |
| A1 | 0.38 | | | 0.015 | | |
| A2 | 3.71 | 3.91 | 4.11 | 0.146 | 0.154 | 0.162 |
| B | 0.36 | 0.46 | 0.56 | 0.014 | 0.018 | 0.022 |
| B1 | 1.02 | 1.27 | 1.56 | 0.040 | 0.050 | 0.065 |
| C | 0.20 | 0.25 | 0.33 | 0.008 | 0.010 | 0.013 |
| D | 36.58 | 37.14 | 37.34 | 1.440 | 1.462 | 1.470 |
| D1 | 0.13 | | | 0.005 | | |
| E | 15.24 | | 15.88 | 0.600 | | 0.625 |
| E1 | 13.64 | 1.89 | 14.15 | 0.537 | 0.547 | 0.557 |
| e | | 2.54 | | | 0.100 | |
| L | 3.18 | | 4.06 | 0.125 | | 0.160 |
| eB | 15.88 | | 16.89 | 0.625 | | 0.665 |

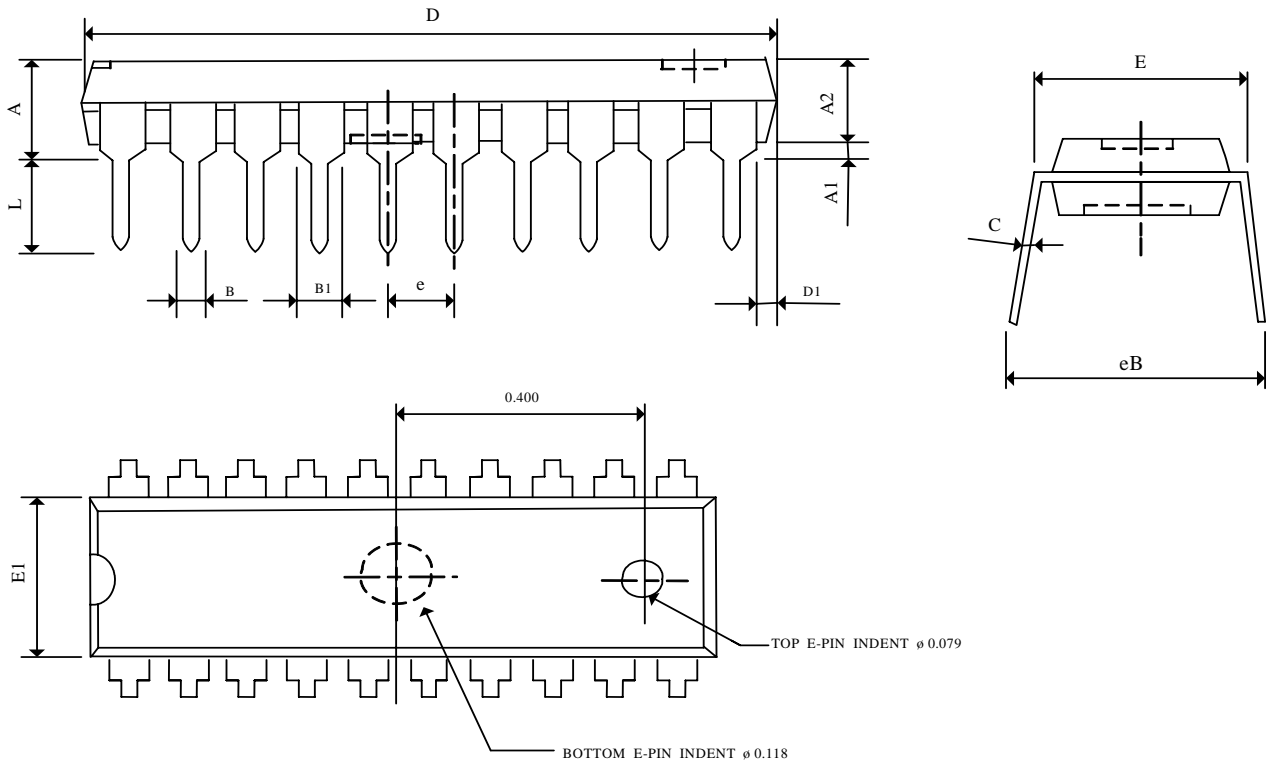


(b) 28 Pin SOP





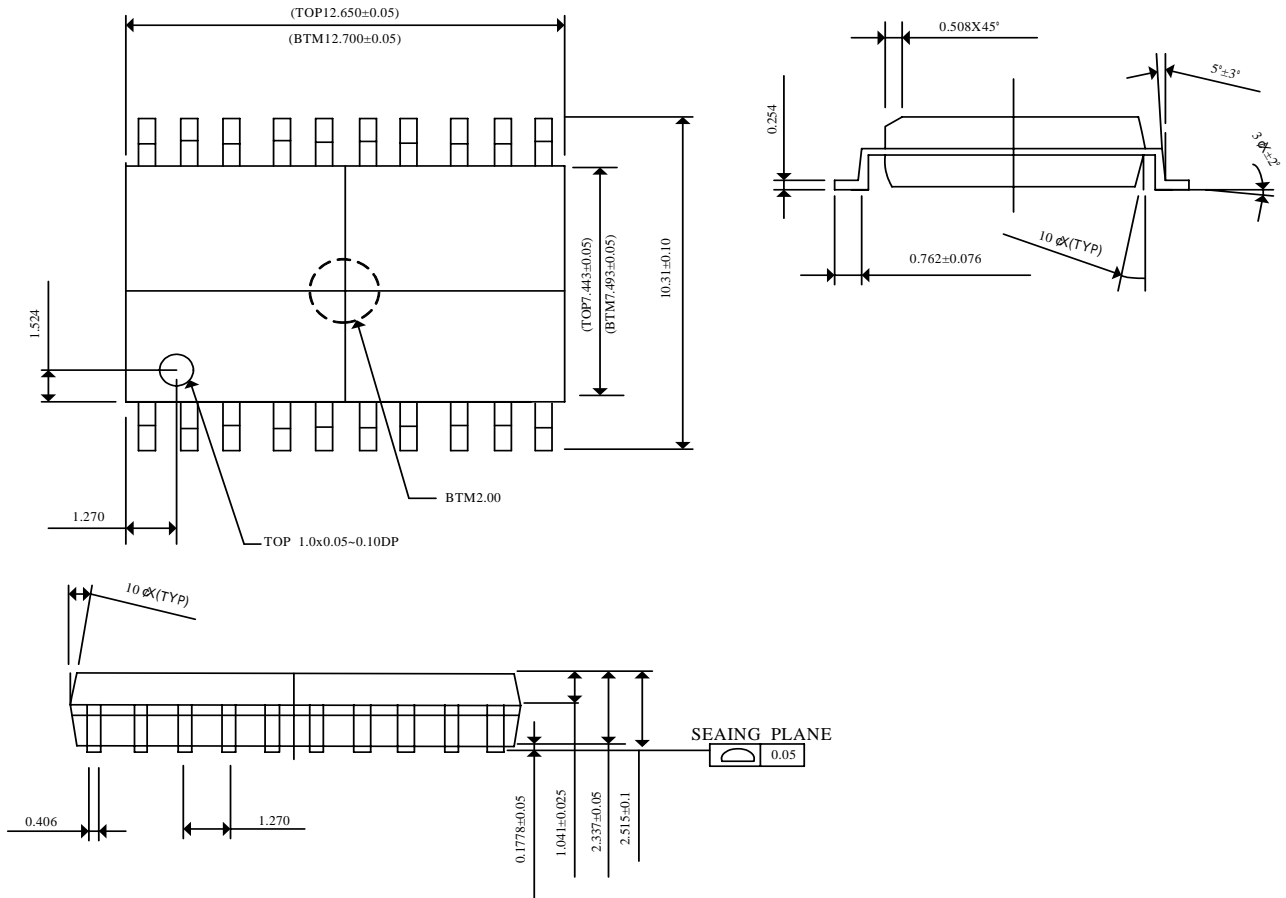
(c) 20 Pin DIP



| SYMBOLS | DIMENSIONS IN MILLIMETERS | | | DIMENSIONS IN INCHES | | |
|---------|---------------------------|-------|-------|----------------------|-------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | | | 4.57 | | | 0.180 |
| A1 | 0.38 | | | 0.015 | | |
| A2 | | 3.30 | 3.56 | | 0.130 | 0.140 |
| B | 0.36 | 0.46 | 0.56 | 0.014 | 0.018 | 0.022 |
| B1 | 1.27 | 1.52 | 1.78 | 0.050 | 0.060 | 0.070 |
| C | 0.20 | 0.25 | 0.33 | 0.008 | 0.010 | 0.013 |
| D | 26.32 | 26.42 | 26.52 | 1.036 | 1.040 | 1.044 |
| D1 | 0.43 | 0.56 | 0.69 | 0.017 | 0.022 | 0.027 |
| E | 7.62 | | 8.26 | 0.300 | | 0.325 |
| E1 | 6.40 | 6.50 | 6.65 | 0.252 | 0.256 | 0.262 |
| e | | 2.54 | | | 0.100 | |
| L | 3.18 | | | 0.125 | | |
| eB | 8.38 | | 9.65 | 0.330 | | 0.380 |

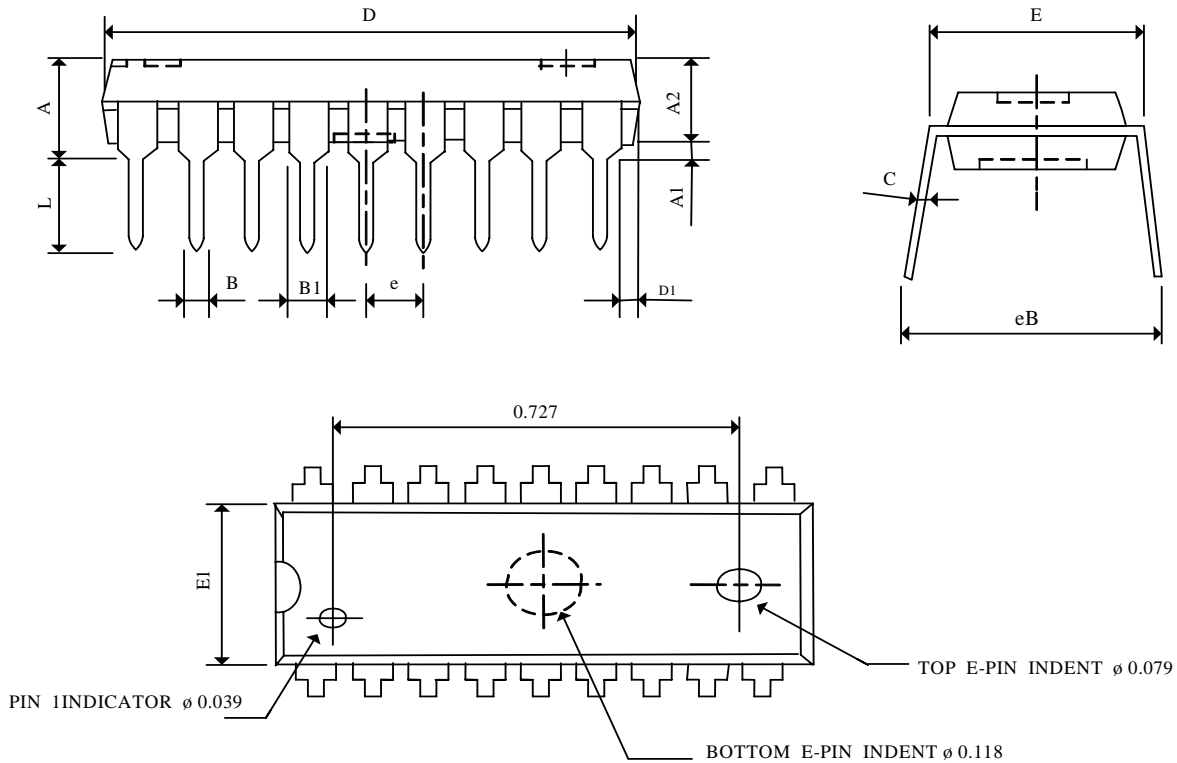


(d) 20 Pin SOP





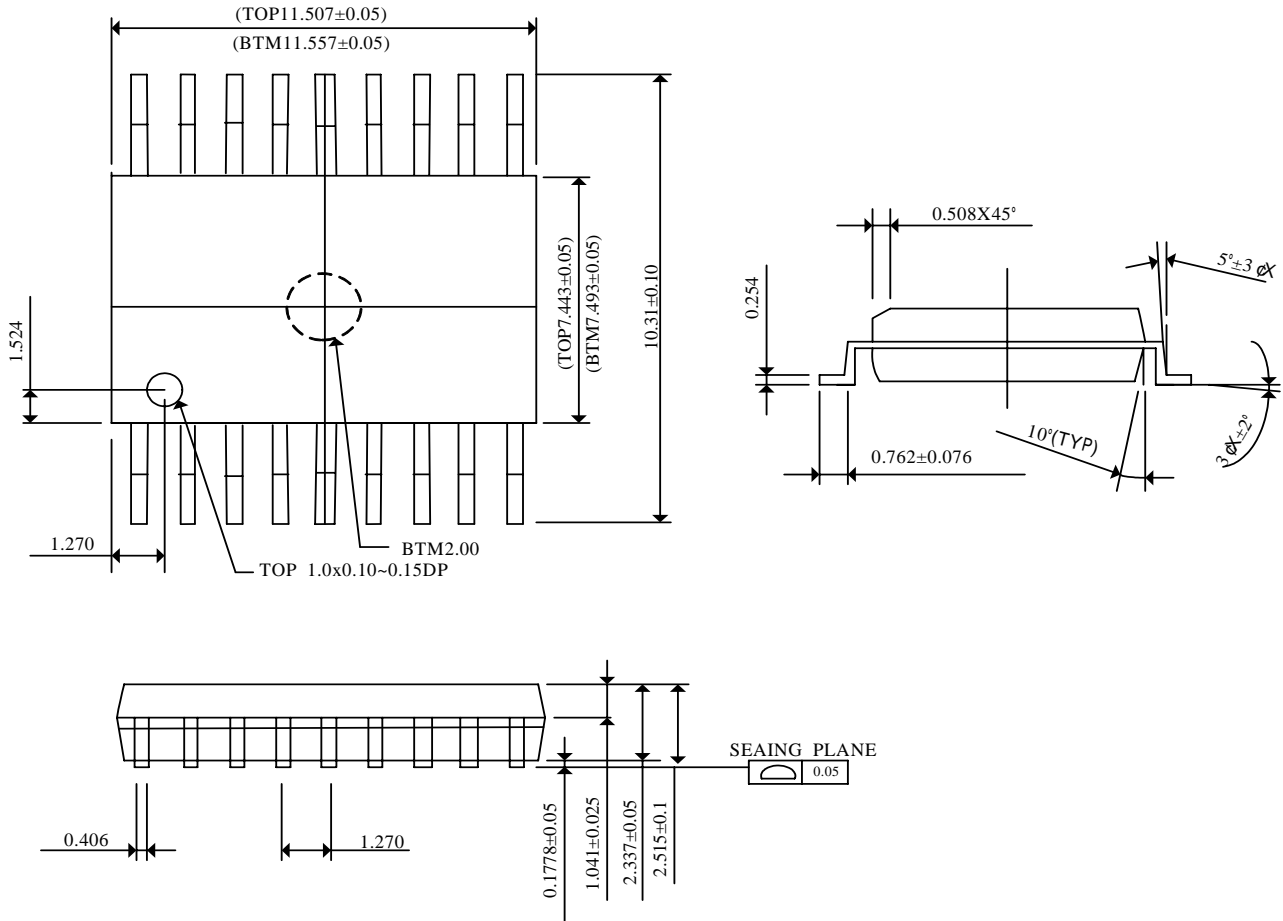
(e) 18 Pin DIP



| SYMBOLS | DIMENSIONS IN MILLIMETERS | | | DIMENSIONS IN INCHES | | |
|---------|---------------------------|-------|-------|----------------------|-------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | | | 4.57 | | | 0.180 |
| A1 | 0.38 | | | 0.015 | | |
| A2 | | 3.30 | 3.56 | | 0.130 | 0.140 |
| B | 0.36 | 0.46 | 0.56 | 0.014 | 0.018 | 0.022 |
| B1 | 1.27 | 1.52 | 1.78 | 0.050 | 0.060 | 0.070 |
| C | 0.20 | 0.25 | 0.33 | 0.008 | 0.010 | 0.013 |
| D | 22.71 | 22.96 | 23.11 | 0.894 | 0.904 | 0.910 |
| D1 | 0.43 | 0.56 | 0.69 | 0.017 | 0.022 | 0.027 |
| E | 7.62 | | 8.26 | 0.300 | | 0.325 |
| E1 | 6.40 | 6.50 | 6.65 | 0.252 | 0.256 | 0.262 |
| e | | 2.54 | | | 0.100 | |
| L | 3.18 | | | 0.125 | | |
| eB | 8.38 | | 9.65 | 0.330 | | 0.380 |



(f) 18 Pin SOP





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