芯睿科技股份有限公司 mikkon technology limited	Total page	8
	Doc No	MK9A35EP AP
	Rev.	0.5

文件名稱	MK9A35BP AP note

版次	生效日	ECN No.	制修訂者	修訂內容概要
0.1	99.3.8		李崑旭 (Jemmy)	新頒。
0.2	2010.3.23		Jemmy	P5~8 Key , LCD & Idd
0.3	2010.7.13		Jemmy	
0.4	2010.8.23		Jemmy	P3 2.40 < LVD < 2.75V
0.5	2010.10.13		Jemmy	P8 STATUS bit6 CORE_VDD 使用限制

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1. MK9A35EP & MK9A35BP & MK9A35P

Modify

	MK9A35EP MK9A35BP	MK9A35P	
ACC (3Fh)	OK	Don't use	
TABRDL	OK	Insert NOP	
TABRDH	OK	Insert NOP	
RFC PAD	OK		
PD4 pull-down	OK	PD3 pull-down control	

IDD

	MK9A35BP MK9A35EP	MK9A35P	
Min. IDD	1.4uA	2.5uA	VDD=3V

2. LVR & LVD

2010.9 LVD 部分測試加測 2.56V 這一階, 範圍 2.45~2.70

不過考量儀表的誤差, spec. 範圍訂為 2.40~2.75V

V_{LVD1}	LVD voltage	3V	SYS_CTL bit4.3=01		2.68		V
V_{LVD2}	LVD voltage	3V	SYS_CTL bit4.3=10		2.42		V
V_{LVD3}	LVD voltage	3V	SYS_CTL bit4.3=11	2.40	2.56	2.75	V

SYS_CTL ($3Eh)

		Low voltage detector	MK9A35BP	MK9A35P
4~3	LVD1~0	1 1	ON (2.56V)	ON (2.6V)
		1 0	ON (2.4V)	ON (2.4V)
		0 1	ON (2.68V)	ON (2.3V)
		0 0	Function OFF	Function OFF

CONFIG (LV1.LV0)

4~3	LV1~0	Low voltage reset	MK9A35BP	MK9A35EP	MK9A35P
		1 1	Don't use	XX	Don't use
		1 0	ON (2.0V)	Fixed (idd=0.3uA)	2.1V
		0 1	ON (1.5V)	XX	Unimplemented
		0 0	ON (1.7V)	XX	Unimplemented

3. Other NEW FUNCTION

	MK9A35BP,MK9A35EP	***MK9A35P***	
Duty	***1/2,1/3*** ***1/4,1/5,1/6,1/7***	***1/4,1/5,1/6,1/7***	
LCD	***1/3 bias*** ***2 LED modes***	***1/3 bias***	
High speed internal RC	***700K & 1.5Mhz***	***700K***	
PA_CTL	***XX (remove)***	***KI function***	
PD_CTL	***Bit 7~0***	***Bit 4,3***	***Key input***
STROBE	***BIT 7,6***		***Key polling mode***
STATUS	***BIT 6,5***		***Low power control***
TM0_CTL	***FCLK,PH0,PH0x2,PH6***	***FCLK,PH0x2***	***Timer 0 source***
4-key reset	***Wdtchdog timer on or off***	***Wdtchdog timer off***	

4. Key matrix (MK9A35E,MK9A50 & MK9A80 & MK9A160)

	MK9A50	*MK9A35EP*	*MK9A80*	*MK9A160*
STROBE	*(1)*	*(2)*	*(2)*	*(2)*
I/O pull-down	*100K*	*100K*	*100K*	*100K*
Key strobe Pull-down	*100K*	*10K*	*10K*	*10K*

STROBE(1)

MK9A50： STROBE($34h)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STROBE	KIEN1	KIEN0	KOAEN	KOEN	KO3	KO2	KO1	KO0

- Bit7~6 (KIEN1~0): Key mode select

Bit \value	11	10	01	00
KIEN1~0	Hardware mode 2	Hardware mode 1	Software mode	OFF

MODE/FUNCTION	SEG1~16	PORT PA0~6 & PC0~7	PORT PD3~4	IRQ
Hardware mode 2	X	Pull down enable	X	V
Hardware mode 1	Hi output	Pull down enable	X	V
Software mode	X	Pull down enable	Pull down enable	X
KOAEN	SEG1~16 : Hi output	X	X	X
KOEN	SEGn : Hi output Others : Floating	X	X	X

(1)省電. 有 IRQ 可以使用

(2)Key (or I/O) Pull-down resister =100K

STROBE(2)

MK9A35E/MK9A80/MK9A160 STROBE ($34h)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STROBE	FRAME	EN	KOAEN	KOEN	KO3	KO2	KO1	KO0

MODE/FUNCTION	SEG1~16	PORT PD[0~7] & PC[0:1]	PORT PA[0~6]
EN	X	Pull down enable	Can't connect to SEGn
KOAEN	SEG1~16 : Hi output	X	X
KOEN	SEGn : Hi output Others : Floating	X	X

(1) Bit7 Frame : read only

(2) Software mode only

(3) Frame=1 時, 讀 key 會比較省電

(3) Mk9A35E/MK9A80 :Key Pull-down=10K,
I/O pull-down=100K

當 **key** 的內阻大於 **2K** 時,會認不到 **key.**

(4)Mk9A160 :Key Pull-down & I/O pull-down=100K

5. LCD/LED (MK9A35E,MK9A50 & MK9A80 & MK9A160)

LCD2~0	*MK9A50*	*MK9A35EP*	*MK9A80*	*MK9A160*
X 0 0	*1/3 bias*	*1/3 bias*	*1/3 bias*	*1/3 bias*
X 0 1	*Led 3*	*1/2 bias #*	*1/2 bias*	*1/2 bias*
X 1 0	*Led 2*	*Led 2*	*Led 2*	*Led 2*
X 1 1	*Led 1*	*Led 1*	*Led 1*	*Led 1*
1 0 0	*x*	*x*	*x*	*1/4 bias*
Duty 1/N	*4,5,6,7,8*	*2,3,4,5,6,7*	*2,3,4,5,6,7,8*	*2,3,4,5,6,7,8, 10,12,16*

(1) MK9A35E/50/80 : 沒有 LCD2 這個 bit

(2) MK9A50 Led3 : ICE 上必須要放 100-pin MK9A50 display.

(3) MK9A35E 1/2 bias 波形與 MK9A80/160 不同,
某些玻璃會有殘影, 使用此功能必須使用 100-pin MK9A35E display.

(4) VDD2 接 VDD 時,
1/2 bias : VDD1=VDD/2 , VDD2=VDD3=VDD4=VDD
1/3 bias : VDD1=VDD/2 , VDD2=VDD, VDD3=VDD4=VDD *3/2
1/4 bias : VDD1=VDD/2 , VDD2=VDD, VDD3=VDD*3/2,
VDD4=VDD * 2.

6. Idd (MK9A35E,MK9A50 & MK9A80 & MK9A160)

省電模式的設定

	MK9A50	MK9A35EP	MK9A80	MK9A160
STATUS bit6	x	Bit6=1 (1)	Bit6=1	Bit6=1
LV	1.5,1.7& 2V	2V (fix)	2V (fix)	1.5,1.7& 2V
Config bit12	x	bit12=1	bit12=1	bit12=1
LCD_CTL bit5.4	Bit5.4=11	Bit5.4=11	Bit5.4=11	Bit5.4=11
Idd (no LVR)	2uA	--	--	1.1uA
Idd (include LVR)	2.3uA	1.7uA	1.4uA	1.4uA
LVR	0.3uA	0.3uA	0.3uA	0.3uA

(1) 9A35EP status bit6=1 只限於 LP mode 使用

7. CORE_VDD (MK9A35EP.MK9A80P,MK9A160P)

STATUS

Bit	Symbol	Description
6	CPU_VDD	CPU_VDD: Internal CORE voltage switch (3V mode) 1: 1.5V 0: 3V

	CPU_VDD=1
Internal 1.5Mhz	VDD1 > 1.3V
Internal 700Khz	VDD1 > 1.2V
Internal 32Khz	VDD1 > 1.1V