芯睿科技股份有限公司
mikkon technology limited

MK9A35FP

(Low power 8bit Microcontroller)

USER'S MANUAL

Table of Content

1. Product Overview

1.1 Feature

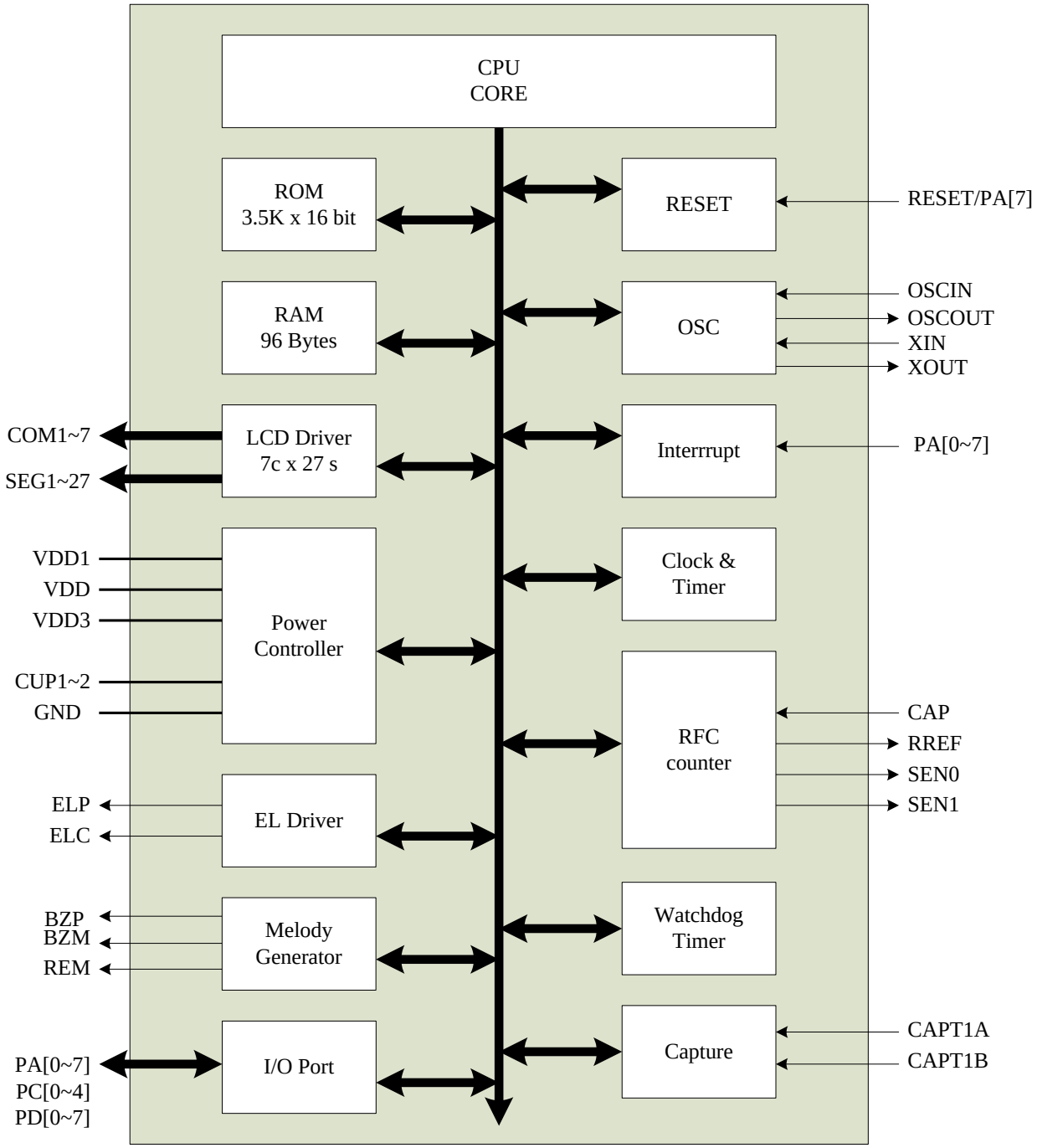
- ROM size: 3.5K * 16 bits
- RAM size: 96 * 8 bits
- Stack: 8 layers
- LCD Driver: 7com * 27seg
  - Duty: 1/2,1/3, 1/4,1/5,1/6 ,1/7 can be selected by register
  - 1/3 bias charge pump, 2 LED modes.
  - COM5~7 can be selected as I/O Port.
- I/O port: 20 bi-direction I/O port, 1 input port.
  - PA[0-6] can be set to pull-up, pull-down , normal output or pmos open-drain or nmos open-drain
  - PA7 input only with pull-down.
  - PC[0-4] can be set to pull-down, normal output or pmos open-drain.
  - PD[0-7] can be set to pull-down, normal output or pmos open-drain.
- Hardware scan key function - normal & halt mode use only.
  - Polling mode : PC[0-1] & PD[0-7]
- SEGn key matrix PC[0-1] & PD[0-7]
- One external interrupt pin which can be set to pull-up, pull-down or high-Z - PD[5]
- Pin-change interrupt
  - Global pins : PA[0-7]
  - Single pin : PD[5]
- System Clock: Dual clock operation

  -Low speed -> External 32KHz Crystal , external R oscillator or 110KHz internal RC oscillator by configuration option

  -High speed -> External 4MHz crystal, external R oscillator or (580KHz, 1.25MHz) internal RC oscillator by configuration option
- Timer0 (TM0) :
  - One 8 bit general purpose timer
  - Remote output (include REM carrier)
  - TM2 & 3 RFC timer base input
- TIMER2 + 3(TM2+3):
  - Two 8-bit timer : TM2 & TM3
  - One 16-bit timer : TM2(high byte) + TM3 (low byte)
  - Two 8-bit Capture/RFC : TM2(high byte) + TM3 (low byte)
  - One 16-bit Capture/RFC : TM2(high byte) + TM3 (low byte)
  - Three 8-bit PWM : TM2,TM3 or (TM2 + TM3)
-

- Other Time base sources
  - PH_IRQ
  - PH_CLK
  - 2Hz
  - One 16 bit pre-divider
  - Watchdog timer
- Watchdog timer & 4'key reset function
  - CONFIG WDTE=0 : 4'key reset enable & watchdog timer disable
  - CONFIG WDTE=1 : 4'key reset disable & watchdog timer enable
- Built-in one RFC channel - CAP, REF , SEN0 & SEN1
- IRQ sources : 7
- Build-in one PWM output - PWM2
- Build -in two capture input - CAPT1A , CAPT1B
- Multi-function (BZ,BZM)output - Tome , FREQ, 1Khz,2Khz,4Khz,PWM2 or PWM3 output
- Built-in EL driver circuit
- Built-in programmable Tone & **REM** output.
- Built-in Low Voltage Reset (LVR) – 1.9V
- Built-in Low Battery Detect -- 2.66V, 2.43V, 2.58V
- Built-in fast reset circuit
- REM - Remote output.
- HALT and SLEEP operation mode
- Fast instruction cycle time: 61us@32KHz operating
- Low power consumption: 5.5uA (@ 32KHz ON,Halt mode , LCD on, No load)

1.2 Block Diagram

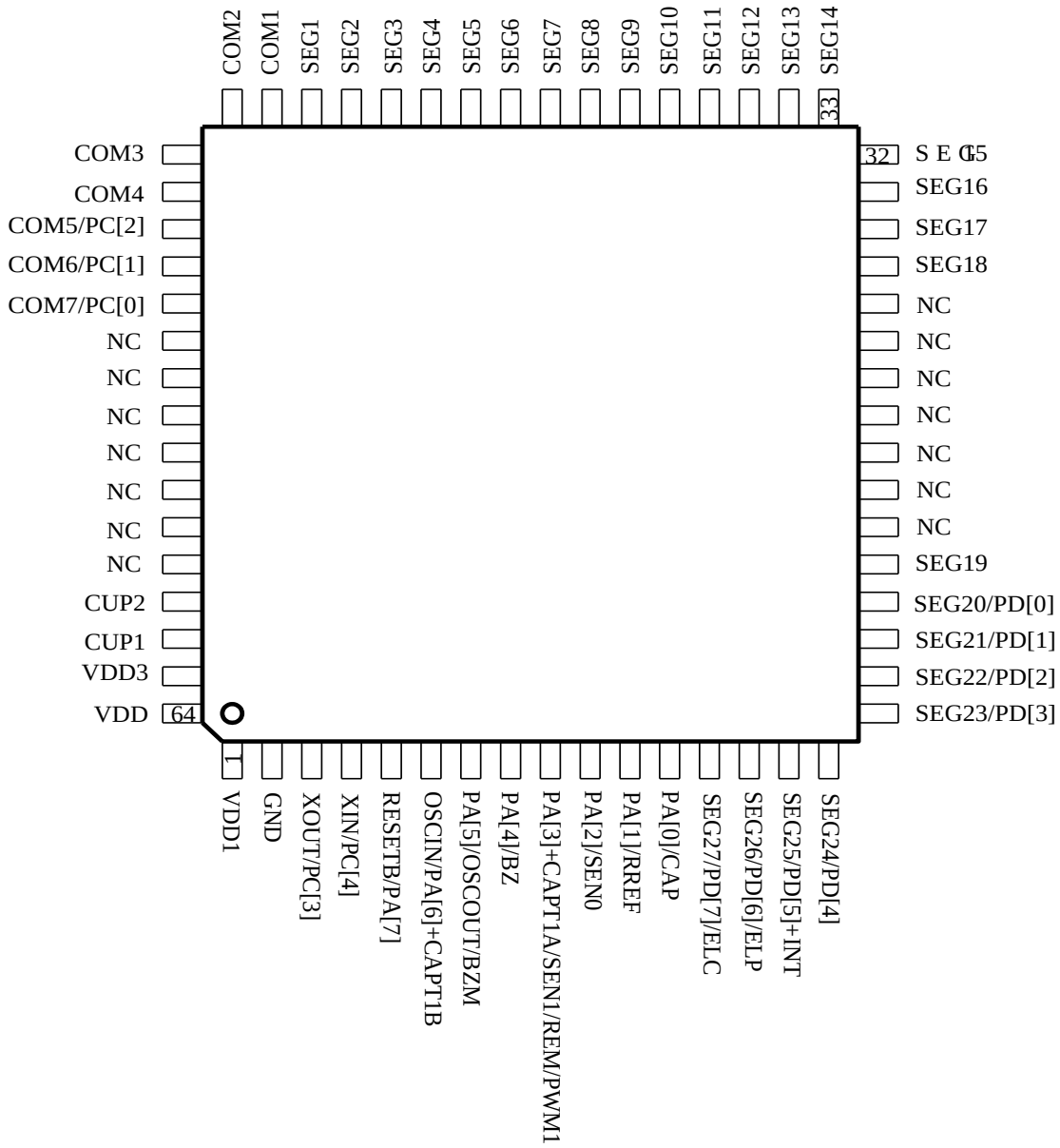


1.3 Pin Assignment

(Pin assignment for COB)

No	Name	No	Name
1	CUP2/VLCD1	27	SEG19
2	CUP1/VLCD2	28	SEG18
3	VDD3	29	SEG17
4	VDD	30	SEG16
5	N.C.	31	SEG15
6	VDD1	32	SEG14
7	N.C.	33	SEG13
8	GND	34	SEG12
9	XOUT/PC[3]	35	SEG11
10	XIN/PC[4]	36	SEG10
11	RESETB/PA[7]	37	SEG9
12	OSCIN /PA[6]+CAPT1B	38	SEG8
13	PA[5]/OSCOUT/BZM	39	SEG7
14	PA[4]/BZ	40	SEG6
15	PA[3]+CAPT1A/SEN1/REM/PWM1	41	SEG5
16	PA[2]/SEN0	42	SEG4
17	PA[1]/RREF	43	SEG3
18	PA[0]/CAP	44	SEG2
19	SEG27/PD[7]/ELC	45	SEG1
20	SEG26/PD[6]/ELP	46	COM1
21	SEG25/PD[5]+INT	47	COM2
22	SEG24/PD[4]	48	COM3
23	SEG23/PD[3]	49	COM4
24	SEG22/PD[2]	50	COM5/PC[2]
25	SEG21/PD[1]	51	COM6/PC[1]
26	SEG20/PD[0]	52	COM7/PC[0]

(LQFP 64-pin)


COM2
COM1
SEG1
SEG2
SEG3
SEG4
SEG5
SEG6
SEG7
SEG8
SEG9
SEG10
SEG11
SEG12
SEG13
SEG14
33
COM3
COM4
COM5/PC[2]
COM6/PC[1]
COM7/PC[0]
NC
NC
NC
NC
NC
NC
NC
NC
CUP2
CUP1
VDD3
VDD
64
32
SEG15
SEG16
SEG17
SEG18
NC
NC
NC
NC
NC
NC
NC
SEG19
SEG20/PD[0]
SEG21/PD[1]
SEG22/PD[2]
SEG23/PD[3]
1
VDD1
GND
XOUT/PC[3]
XIN/PC[4]
RESETB/PA[7]
OSCIN/PA[6]+CAPT1B
PA[5]/OSCOUT/BZM
PA[4]/BZ
PA[3]+CAPT1A/SEN1/REM/PWM1
PA[2]/SEN0
PA[1]/RREF
PA[0]/CAP
SEG27/PD[7]/ELC
SEG26/PD[6]/ELP
SEG25/PD[5]+INT
SEG24/PD[4]

1.4 Pin Description

Pin name	I/O	Description
PA[0]/CAP	I,I/O	1. Input port with pull up, pull down or pin wake up 2. Output port (Normal output, P open drain or N open drain) 3. CAP input
PA[1]/REF	I,I/O	1. Input port with pull up, pull down or pin wake up 2. Output port (Normal output, P open drain or N open drain) 3. REF output
PA[2]/SEN0	I,I/O	1. Input port with pull up, pull down or pin wake up 2. Output port (Normal output, P open drain or N open drain) 3. SEN0 output
PA[3]+CAPT1A/SEN1/ REM/PWM1	I,I/O	1. Input port with pull up, pull down or pin wake up 2. Output port (Normal output, P open drain or N open drain) 3. CAPT1A input 4. REM output 5. PWM1 output 6. SEN1 output
PA[4]/BZ	I,I/O	1. Input port with pull up, pull down or pin wake up 2. Output port (Normal output, P open drain or N open drain) 3. BZM output
OSCOUT/PA[5]/BZM	I,I/O	1. Crystal out 2. I/O port (pull-high, pull-down, open-drain, pin wake up) 3. BZM output
OSCIN/PA[6]+CAPT1B	O,I/O	1. Crystal in 2. External RC input 3. I/O port (pull-high, pull-down, open-drain, pin wake up) 4. CAPT1B input
RESETB/PA[7]	I,I	1. System reset input 2. Input port with pull-low 3. Wake -up on pin change
XIN/PC[4]	I,O	1. Crystal input (32K) 2. Input port with pull-down 3. PC output port (Normal output or PMOS open-drain)
XOUT/PC[3]	O,O	1. Crystal out 2. Input port with pull-down 3. PC output port (Normal output or PMOS open-drain)
GND	P	System Ground
VDD1,3	P	LCD power supply
VDD	P	System power supply
CUP1	P	Voltage step up capacitor
CUP2	P	Voltage step up capacitor
COM1~4	O	LCD COM output
COM7/PC[0]	O,I	1. LCD COM output 2. Input port (pull-down) 3. PC output port (Normal output or PMOS open-drain) 4. KI input
COM6/PC[1]	O,I	1. LCD COM output 2. Input port (pull-down) 3. PC output port (Normal output or PMOS open-drain) 4. KI input

COM5/PC[2]	O,I	1. LCD COM output 2. Input port (pull-down) 3. PC output port (Normal output or PMOS open-drain)
SEG1~19	O, O	LCD segment output
SEG20/PD[0]	O,O	1. LCD segment output 2. PD input port with pull-down 3. PD output port (Normal output or PMOS open-drain)
SEG21/PD[1]	O,O	1. LCD segment output 2. PD input port with pull-down 3. PD output port (Normal output or PMOS open-drain)
SEG22/PD[2]	O,O	1. LCD segment output 2. PD input port with pull-down 3. PD output port (Normal output or PMOS open-drain)
SEG23/PD[3]	O,O	1. LCD segment output 2. PD input port with pull-down 3. PD output port (Normal output or PMOS open-drain) 4. KI input
SEG24/PD[4]	O,O	1. LCD segment output 2. PD input port with pull-down 3. PD output port (Normal output or PMOS open-drain) 4. KI input
SEG25/PD[5]	O,O	1. LCD segment output 2. PD input port with pull-down 3. PD output port (Normal output or PMOS open-drain) 4. Pin interrupt
SEG26/PD[6]/ELP	O,O	1. LCD segment output 2. PD input port with pull-down 3. PD output port (Normal output or PMOS open-drain) 4. ELP output
SEG27/PD[7]/ELC	O,O	1. LCD segment output 2. PD input port with pull-down. 3. PD output port (Normal output or PMOS open-drain) 4. ELC output

2. System Architecture

2.1 System Clock

The MK9A35FP has dual clock operation mode and user can set bit0~3 of configuration register to be their request. OSCIN/OSCOUT, which we call fast clock, can be used to connect external NT mode crystal, external R oscillator or internal 580KHz RC oscillator by configuration option. When user select internal 580KHz RC oscillation mode, these two pins can be used as KI or I/O ports (PA) that is more flexibility. XIN/XOUT, which we call slow clock, has the same situation. They can be used to connect external LP mode crystal or internal 110KHz RC oscillator. When user select internal 110KHz RC oscillator, these two pin can be used as I/O ports (PB). The clock mode can be selected by configuration bit. Once dual clock mode is selected, user can switch between fast and slow clock by setting bit 7 of SYS_CTL ($3Eh). Or turn on/off these clock source individually by setting bit0~1.

The clock oscillation block diagram is as below which is composed of fast clock and slow clock.

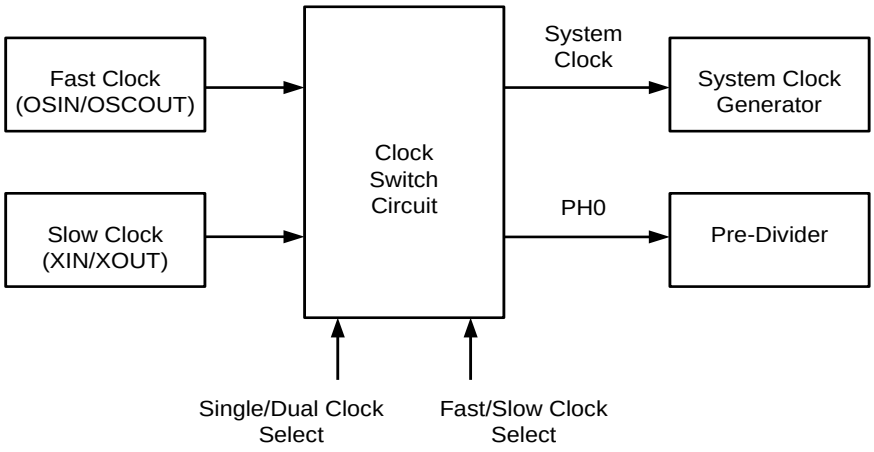


Fig.2.1.1 System clock & Pre-divider

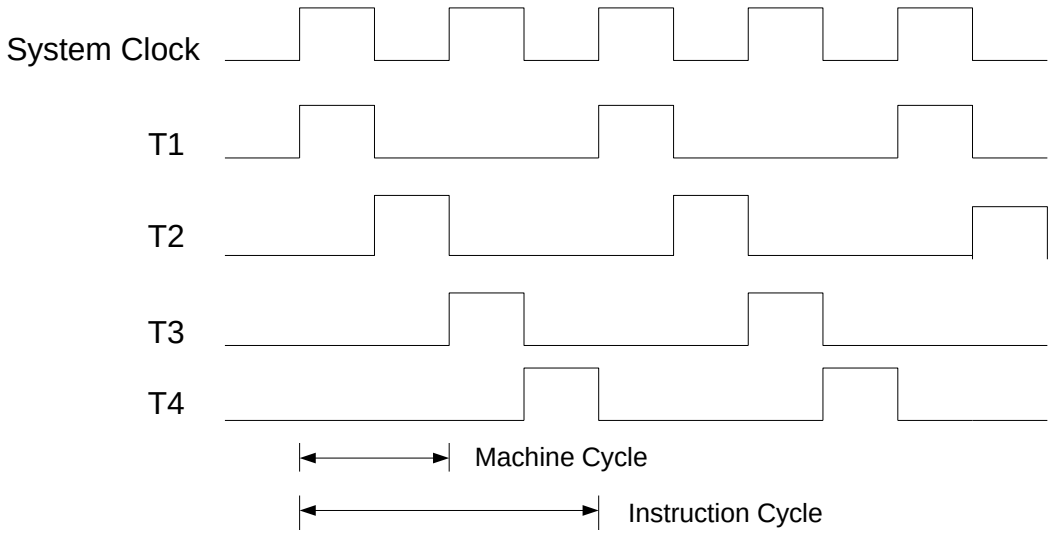


Fig.2.1.2 Machine Cycle & Instruction Cycle

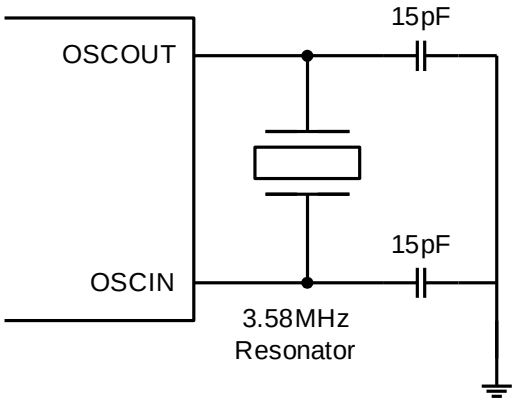
The below table shows the clock source status of system clock and pre-divider in different mode:

Clock Mode	System Clock	PH0
Slow Clock Only	SCLK (Slow Clock)	SCLK
Fast Clock Only	FCLK (Fast Clock)	FCLK
Initial Stage (Dual Clock Mode)	SCLK	SCLK
HALT Stage (Dual Clock Mode)	SCLK	SCLK
Slow Clock Active (Dual Clock Mode)	SCLK	SCLK
Fast Clock Active (Dual Clock Mode)	FCLK	SCLK

2.1.1 Fast Clock (FCLK) Connection

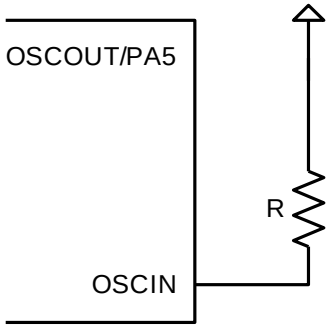
There are 3 connection circuits of fast clock which are external max. 4MHz crystal or resonator, external R oscillator and internal 580KHz RC oscillator. User can select the operation mode by setting configuration register bit 2~3. The connection are as below drawing:

甲、 Connect external 3.58MHz Resonator, (FOSC1,FOSC0)=(0,0)



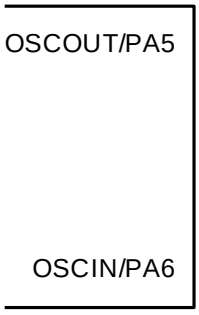
乙、 Connect external R oscillator, (FOSC1,FOSC0)=(1,0)

When set to this mode, OSCOUT pin can be used as I/O port (PA5).



丙、 Fast clock is set to internal RC oscillator or No, (FOSC1,FOSC0)=(1,1) or (0,1)

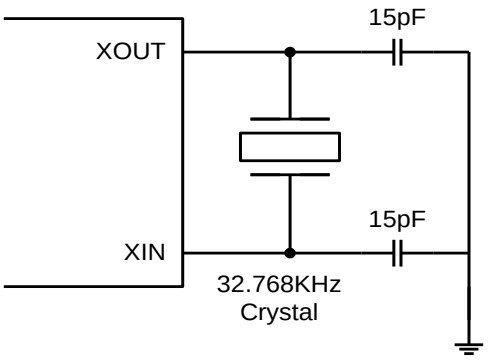
When set to this mode, OSCIN and OSCOUT can be used as I/O port (PA6 and PA5)



2.1.2 Slow Clock (SCLK) Connection

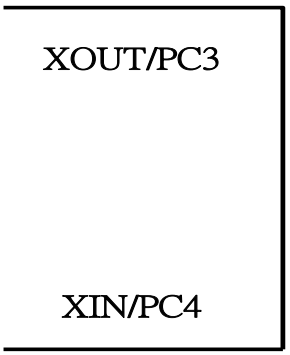
There are 2 connection circuits of fast clock which are external LP mode crystal and internal 110KHz RC oscillator. User can select the operation mode by setting configuration register bit 0~1. The connection are as below drawing:

(a) Connect external 32.768KHz Crystal, (SOSC1,SOSC0)=(0,0)



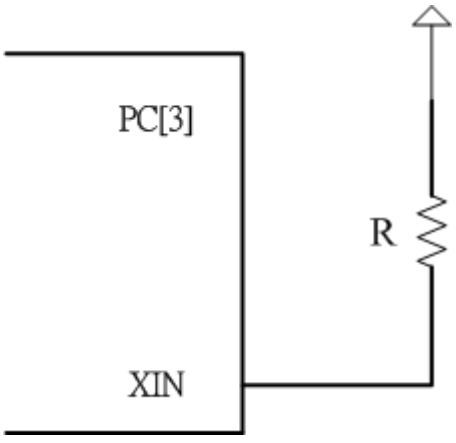
(b) Slow clock is set to internal RC oscillator or No, (SOSC1,SOSC0)=(1,1) or (0,1)

When set to this mode, XIN and XOUT can be used as output ports (PC4 and PC3)



(c) Slow clock is set to external RC oscillator (SOSC1,SOSC0)=(1,0)

When set to this mode, XOUT can be used as I/O port (PC3)



FCLK & SCLK switch

2.1.3-1 Cpu clock switch from SCLK to FCLK

```
BC      SYS_CTL,1    ;; enable fast clock , cpu clock = SCLK
NOP                  ;; fast clock stabile time
NOP
NOP
BS      SYS_CTL,7    ;; cpu clock = FCLK
```

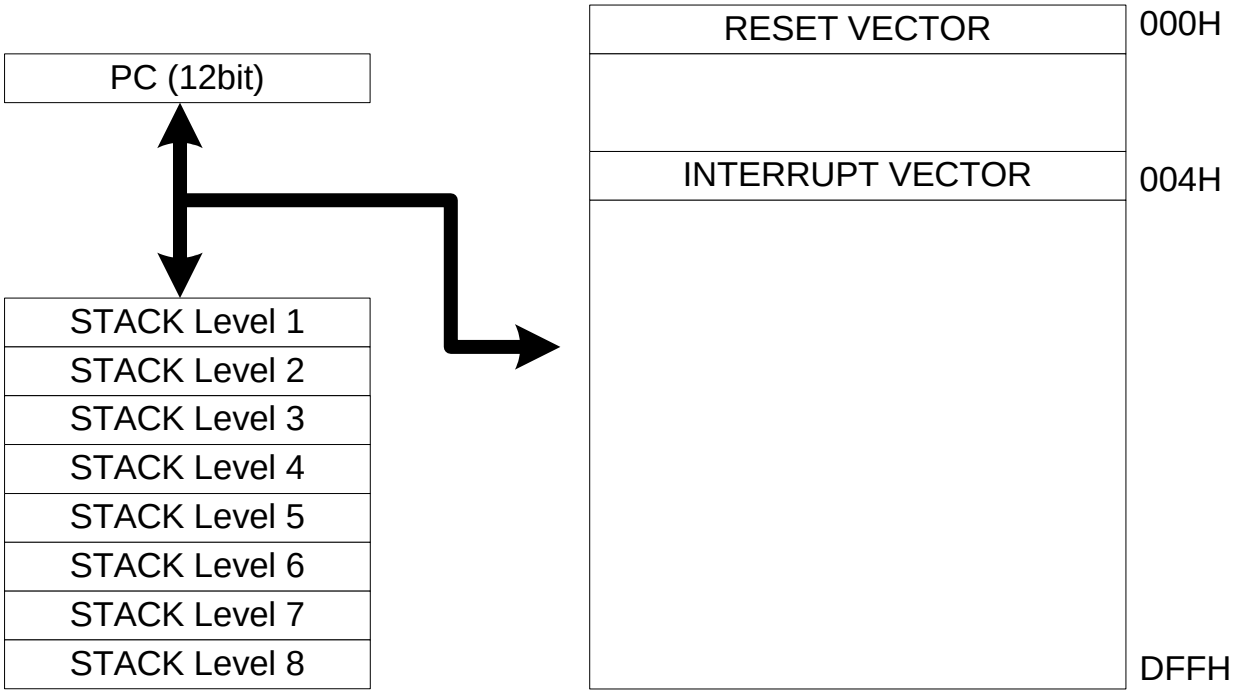
2.1.3-2 Cpu clock switch from FCLK to SCLK

```
                     ;; FCLK & SCLK are all ON , cpu clock = FCLK
BC      SYS_CTL,7    ;; enable fast clock , cpu clock = SCLK
NOP                  ;; fast clock stabile time
NOP
BS      SYS_CTL,1    ;; Stop FCLK
```

2.2 Program Memory (ROM)

Instruction and table are stored at this area. There is only one interrupt vector existed which means all the interrupt occurred would jump to the same vector. Programmer should use interrupt flag to judge what kind of interrupt is occurred. The program counter (PC) is 12 bit which can directly address all the 12K x 16 location. Look-up table can be put at anywhere of ROM.

The RESET vector is located at 000H and Interrupt vector is at 004H. The map is as below



2.3 Data Memory (RAM)

The total RAM volume are 160 x 8bits which includes three kinds of register group. One is 96 × 8bits working RAM, another is special purpose register that are 37 × 8bits and display RAM are 27 x 8bits. The data memory map is as below:

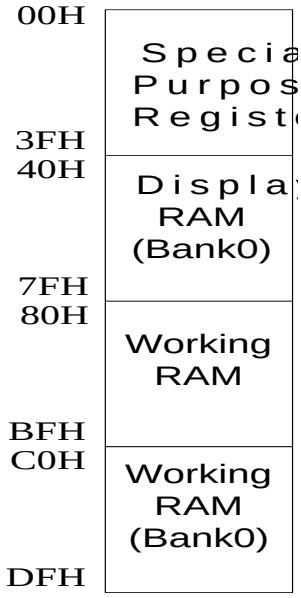


Fig.2.3.1 Memory mapping

User can set WBANK register to switch different bank of data RAM. The definition is as below:

2.4 Configuration Register

This register store set up option of chip which includes reset pin definition, timer clock source select, LVR detect voltage select and WDT control. The content of register can not be changed by software and will be fixed by Writer. It is like mask option when use mask ROM type MCU.

Register	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
CONFIG_L	LV1	LV0	WDTE	CPT	FOSC1	FOSC0	SOSC1	SOSC0
-	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
CONFIG_H	--	--	--	POWER	-	RSTE2	RSTE1	RST_DEF

- Bit 12 : Low control control
  1 : Low power control ON
  0 : Low power control OFF

- Bit 10~9 (RSTE2.1): PA 2'S 4-KEY reset number control (Only PA work as I/O mode)
  When press PA keys over 2 secs, Reset Occurred
  1 1 : max. 4-key reset (4 key depress simultaneously) -- PA7,PA6,PA5,PA3
  1 0 : max. 4-key reset (4 key depress simultaneously) -- PA7,PA5,PA4,PA3
  0 1 : max. 4-key reset (4 key depress simultaneously) -- PA6,PA5,PA4,PA3
  0 0 : max. no key reset

KI/IO	WDTE.RSTE2~1	2'S 4-key reset RESET pins function	RESET pins				
			PA3	PA4	PA5	PA6	PA7
KI	XXX	No key reset function	X	X	X	X	X
IO	1 X X	No key reset function	X	X	X	X	X
IO	0 0 0	No key reset function	X	X	X	X	X
IO	0 0 1	PA7,PA6,PA5,PA3	ON	X	ON	ON	ON
IO	0 1 0	PA7,PA5,PA4,PA3	ON	ON	ON	X	ON
IO	0 1 1	PA6,PA5,PA4,PA3	ON	ON	ON	ON	X

<Note> To use this key reset function, PA should be set as I/O port at first in PAD_CTL2($14) register and set PA as input pull-high in normal operation mode. When use this function and enter SLEEP mode, the specific PA port would automatically set as pull high. For example, if user define PA[3]~PA[4] to be key reset. When system enter SLEEP mode, PA[3] and PA[4] would be set as pull-high. At this moment, user should be careful don't hold these keys down, otherwise that will cause the power consumption.

- Bit8 (RST_DEF): RESETB pin function define
  0: RESETB used as normal I/O Input pin
  1: RESETB used as system reset pin
- Bit7~6 (LV1~0): Low voltage reset function voltage selection bits

Bit7	**Bit6**	**Detect voltage**
LV1	**LV0**	
X	1	Don't use
1	0	1.9V
1	1	Don't use

- Bit5 (WDTE): Watchdog timer enable/disable control
  0: WDT disable (PA 2'S KEY reset function is enable)
  1: WDT enable (PA 2'S KEY reset function is disable)

Bit1~0	**OSC Type**	**Watchdog timer source**
SOSC1~0		
00	**LP (low speed)**	**Internal 110K RC**
01	**No**	**Internal 110K RC**
10	**External RC**	**External RC**
11	**Internal RC**	**Internal 110K RC**

- Bit4 (CPT): Code Protection bit

  0: ON

  1: OFF

- Bit3~2 (FOSC2~1): OSCIN/OSCOUT frequency assignment bit.

Bit3	Bit2	OSC Type	Resonance Frequency
FOSC1	FOSC0		
0	0	NT (Normal speed)	455KHz~10Mhz resonator or crystal
0	1	No	OSCIN & OSCOUT used as I/O port or KI
1	0	External R	1.OSCIN connect to R (455KHz~4MHz) 2. OSCOUT can be used as I/O port
1	1	Internal RC	1. Internal (580KHz, 1.25MHz) RC oscillator 2. OSCIN & OSCOUT can be used as I/O port

- Bit1~0 (SOSC1~0): XIN/XOUT frequency assignment bit.
-

Bit1	Bit0	OSC Type	Resonance Frequency
SOSC1	SOSC0		
0	0	LP (low speed)	32KHz crystal
0	1	No	XIN & XOUT work as I/O port
1	0	External RC	1. External low RC oscillator 2.XOUT can be used as I/O port
1	1	Internal RC	1.Internal 110KHz RC oscillator 2.XIN & XOUT can be used as I/O port

<Note> Below table shows system clock status during Reset stage and CLKS bit setting:

Bit3	Bit2	Bit1	Bit0	System clock			PH0
FOSC1	FOSC0	SOSC1	SOSC0	Reset	CLKS=0	CLKS=1	
0	0	0	0	Slow clock	Slow clock	Fast clock	Slow clock
0	0	0	1	Slow clock only, Can't write "1" to CLKS			Slow clock
0	0	1	X	Slow clock	Slow clock	Fast clock	Slow clock
0	1	0	0	Fast clock only, Can't write "0" to CLKS			Slow clock
0	1	0	1	Don't care			XX
0	1	1	X	Fast clock only, Can't write "0" to CLKS			Fast clock
1	0	0	0	Slow clock	Slow clock	Fast clock	Slow clock
1	0	0	1	Slow clock only, Can't write "1" to CLKS			Slow clock
1	0	1	X	Slow clock	Slow clock	Fast clock	Slow clock
1	1	0	0	Slow clock	Slow clock	Fast clock	Slow clock
1	1	0	1	Slow clock only, Can't write "1" to CLKS			Slow clock
1	1	1	X	Slow clock	Slow clock	Fast clock	Slow clock

2.5 Special Purpose Register

The listed register table is as below, we will describe them in detail at the specific chapter.

Name	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INDF	$00	A7	A6	A5	A4	A3	A2	A1	A0
PCL	$01	A7	A6	A5	A4	A3	A2	A1	A0
PCH	$02	--	--	--	--	A11	A10	A9	A8
STATUS	$03	--	POWER	VOLT	$\overline{TO}$	$\overline{PD}$	Z	DC	C
FSR	$04	BANK1	BANK0	D5	D4	D3	D2	D1	D0
I/O PAD & Control									
Name	**Addr**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
PA_DIR	$05	--	DA6	DA5	DA4	DA3	DA2	DA1	DA0
WAKE_UP	$07	EN7	EN6	EN5	EN4	EN3	EN2	KI1/IN1	EN0
PA_PUD1	$08	A3-2	A3-1	A2-2	A2-1	A1-2	A1-1	A0-2	A0-1
PA_PUD2	$09	A7-2	A7-1	A6-2	A6-1	A5-2	A5-1	A4-2	A4-1
PA_DAT	$0A	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
PC_CTL	$0B	--	--	--	--	--	--	KI1/IN1	KI0/IN0
PC_DIR	$0C	--	--	--	DC4	DC3	DC2	DC1	DC0
PC_PUD	$0D	--	--	--	UC4	UC3	UC2	UC1	UC0
PC_DAT	$0E	--	--	--	PC4	PC3	PC2	PC1	PC0
PD_DIR	$0F	DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0
PD_PUD	$10	UD7	UD6	UD5	UD4	UD3	UD2	UD1	UD0
PD_CTL	$11	KI7/IN7	KI6/IN6	KI5/IN5	KI4/IN4	KI4/IN3	KI2/IN2	KI1/IN1	KI0/IN0
PD_DAT	$12	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
PAD_CTL1	$13	SEG27/ PD[7]	SEG26/ PD[6]	SEG25/ PD[5]	SEG24/ PD[4]	SEG23/ PD[3]	SEG22/ PD[2]	SEG21/ PD[1]	SEG20/ PD[0]
PAD_CTL2	$14	--	C6	C5	C4	C3	C2	C1	C0
PAD_CTL3	$15	EDGE					SEN1_ON	SEN0_ON	REF_ON
TM0: 8-bit Timer (TONE & FREQ out)									
Name	**Addr**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
TM0_CTL	$17	EN	WR_CNT	DATA	**IRQ_S**	SUR1	SUR0	DUTY1	DUTY0
TM0_LA	$18	D7	D6	D5	D4	D3	D2	D1	D0
TM0_CNT	$19	D7	D6	D5	D4	D3	D2	D1	D0
TONE_CTL1	$39	EN	PH15E	PH14E	PH13E	PH12E	PH11E	PAT1	INV12
TONE_CTL2	$3A						CRY2	CRY1	CRY0
TM2 : 8-bit Timer x1 , 8-bit capture x1									

Name	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM2_CTL1	$1F	EN	WR_CNT	BIT	MOD1	MOD0	EDGE	SUR1	SUR0
TM2_CTL2	$20	ENC	CLR_CNT	--	--	CAPIN0/ RFC_T0	INT_S	PWM_OS	OV
TM2_LA	$21	D7	D6	D5	D4	D3	D2	D1	D0
TM2_CNT	$22	D7	D6	D5	D4	D3	D2	D1	D0
TM3_CTL1	$23	EN	WR_CNT		MOD1	MOD0	EDGE	SUR1	SUR0
TM3_CTL2	$24	ENC	CLR_CNT	--	--	CAPIN0/ RFC_T0	INT_S	PWM_OS	OV
TM3_LA	$25	D7	D6	D5	D4	D3	D2	D1	D0
TM3_CNT	$26	D7	D6	D5	D4	D3	D2	D1	D0

Interrupt Control

Name	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CPU_RESUME	$30		PAR	PINTR	2HZR	PHR	TM3R/ PWM3R/ CAPTR/ RFC3R	TM2R/ PWM2R/ CAPTR/ RFC2R	TM0R/ TONER
IRQM	$31	INTM	PAM	PINTM	2HZM	PHM	TM3M/ PWM3M/ CAPT3M/ RFC3M	TM2M/ PWM2M/ CAPT2M/ RFC2M	TM0M/ TONEM
IRQF	$32		PAF	PINTF	2HZF	PHF	TM3F/ PWM3F/ CAPT3F/ RFC3F	TM2F/ PWM2F/ CAPT2F/ RFC2F	TM0F/ TONEF

Other

LBASDT	$33	LCD1	LCD0	FRAM1	FRAM0	--	DUTY2	DUTY1	DUTY0
STROBE	$34	FRAME	EN	KOAEN	KOEN	KO3	KO2	KO1	KO0
LCD_CTL	$35	PUMP1	PUMP0	POW1	POW0	OVP1	OVP0	LCDM1	LCDM0
PH_CTL	$36	ELON	EL_SEL	EL_P	CLR	PH_I1	PH_I0	PH_S1	PH_S0
PH_OUT	$37	PH15	PH14	PH13	PH12	PH11	PH10	PH9	PH8
PH_OUT1	$38	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0
WDT_CTL	$3B	WDTEN	--	--	--	--	PRE2	PRE1	PRE0
TAB_BNK	$3D	--	--	--	--	TBA3	TBA2	TBA1	TBA0
SYS_CTL	$3E	CLKS	HALT	--	LVD1	LVD0	LV	STP1	STP0

2.6 HALT mode Function

HALT function is used to minimize the power consumption of CPU in standby. User can set register $3Eh bit 6 to enter HALT mode in below table. During this stage, CPU operation is off which means the program memory is not in working. Only slow clock, timer and LCD driver blocks are in operation.

SYS_CTL ($3Eh)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SYS_CTL	CLKS	HALT	IRC--	LVD1	LVD0	LV	STP1	STP0

Bit	Symbol	Description	
7	CLKS	System Clock Select (Default is SCLK) 0: Slow clock (SCLK) 1: Fast clock (FCLK)	
6	HALT	CPU on/off control 0: ON 1: CPU OFF (halt mode enable)	
4~3	LVD1~0	Low voltage detector	
		1 1	ON (2.58V)
		1 0	ON (2.43V)
		0 1	ON (2.66V)
		0 0	Function OFF
2	LV	Low power output 0: Power voltage > 2.66V (or 2.43V, 2.58V) 1: Power voltage < 2.66V (or 2.43V, 2.58V)	
1	STP1	Fast clock control (Default is OFF) 0: ON 1: OFF	
0	STP0	Slow clock control (Default is ON) 0: ON 1: OFF	

There are several events can release the HALT mode which are:

(1) Pin change wake up (External interrupt pin PA7~0 ,PD5 ,CAPT1A & CAPT1B)

(2) Timer interrupt (PH ,2Hz,TMR0 , TMR2 & TMR3)

(3) Watchdog timer

(4) Reset

The diagram is as below:

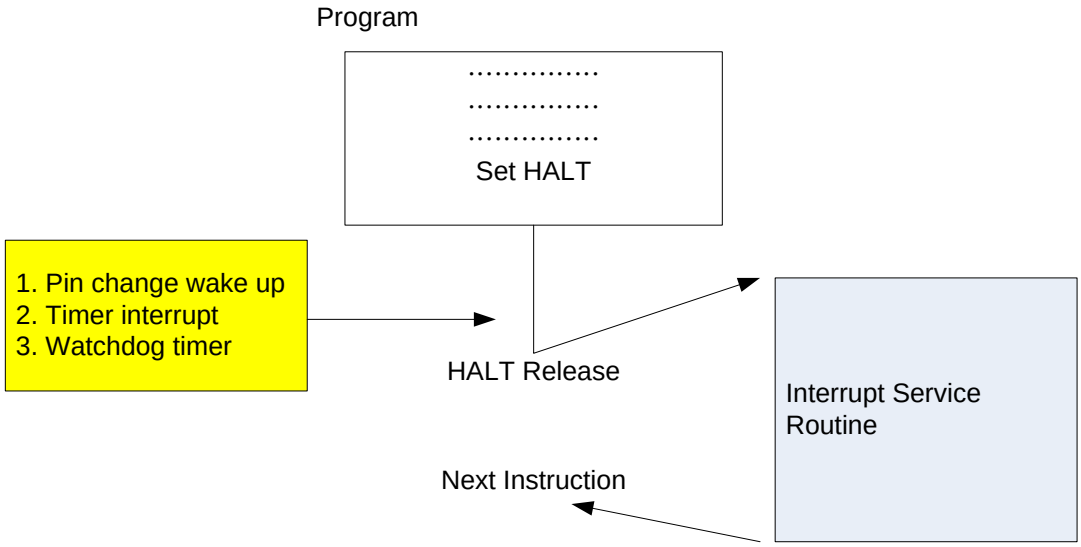


Fig.2.6.1 HALT Release

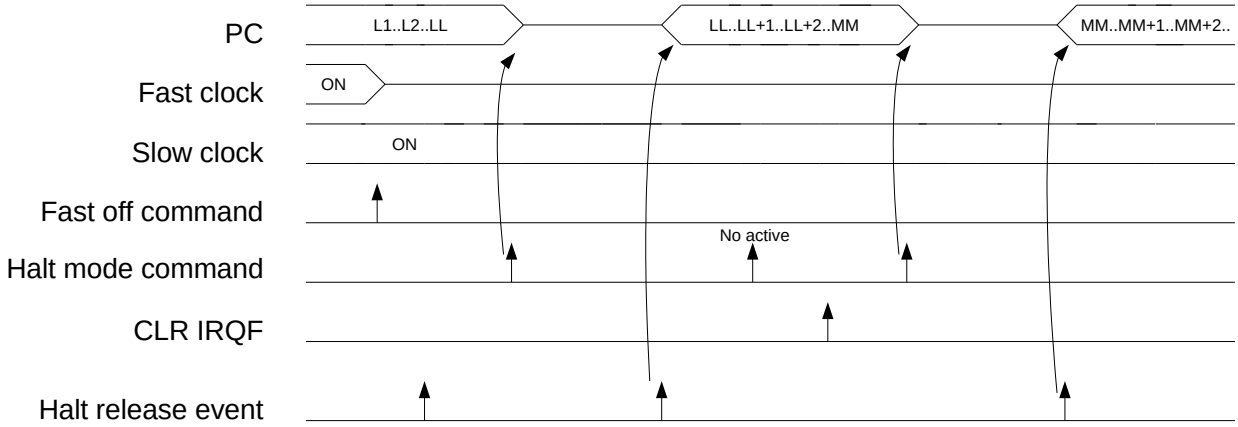


Fig.2.6.2 Halt mode & Halt Release waveform

2.7 SLEEP Function

When system enter the sleep mode by using the instruction SLEEP, all the clocks and circuits (include LCD) will stop operation except watchdog timer and pin change wake up circuit. During this mode, the current consumption is almost zero. Only two events can wake up from SLEEP mode, that are:

(1) Pin change wake up **(External interrupt pin PA7~0 & PD5)**

(2) Capture mode (CAPT1A, CAPT1B)

(3) Watchdog timer

(4) Reset

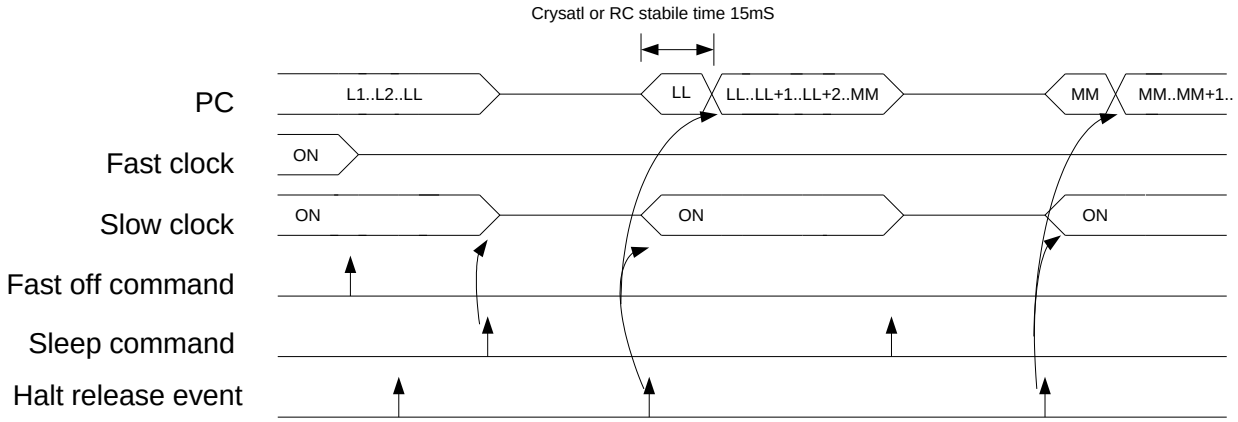


Fig.2.7.1 Sleep & Halt Release waveform

2.8 Table Look-up Function

The MK9A35FP provide table look-up function. The look-up tables can be placed at any location in the ROM space. The instruction of TABRDL is to read low byte of ROM table. And The TABRDH is to read high byte. The register of TAB_BNK and PC[7:0] are used to define starting address of table.

TAB_BNK ($3Dh)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBH	--	--	--	--	TBA3	TBA2	TBA1	TBA0

- Bit3~0 (TBA3~0): High byte table location bits , Table address ={TBA3~0,PC[7:0]}

2.9 FSR: Bank Select Register

This register will be used with INDF register for indirect addressing data memory.

FSR ($04h)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FSR	BANK1	BANK0	D5	D4	D3	D2	D1	D0

Bit	Symbol	Description	
7~6	BANK1~0	Low voltage detector	
		0 0	Special purpose register
		0 1	Display RAM
		1 0	Direct access working RAM (80h~BFh)
		1 1	Direct access working RAM (C0h~DFh)

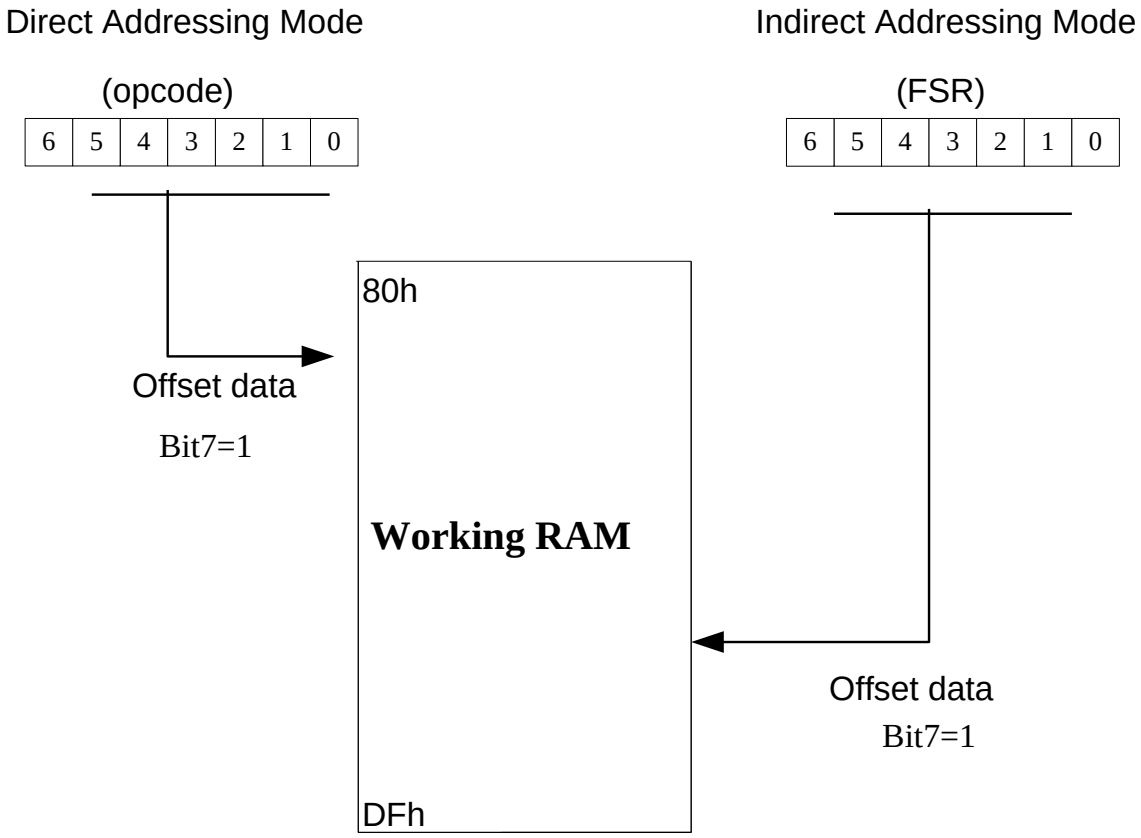


Fig.2.9.1 Working RAM

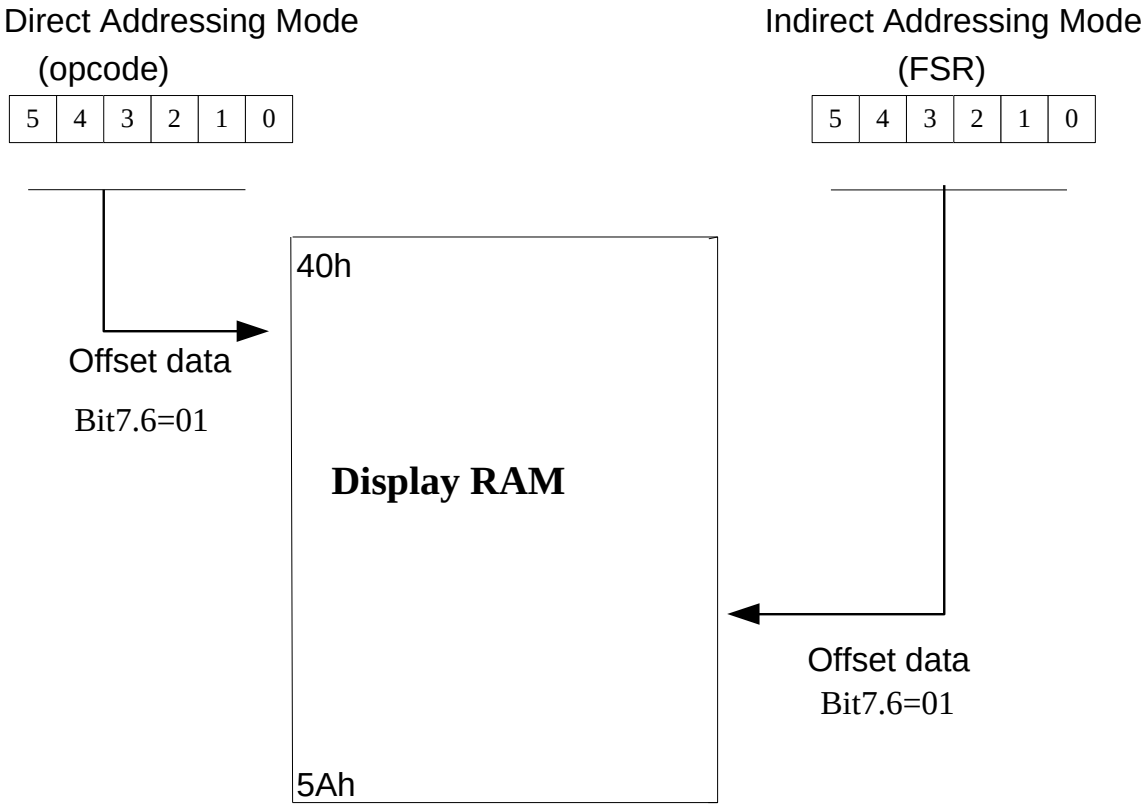


Fig.2.9.2 Display RAM

2.10 Status Register

The STATUS register is an 8-bit register that contains the zero flag (Z), carry flag (C), Nibble carry flag (DC), power down flag ($\overline{PD}$), and watchdog timer overflow flag ($\overline{TO}$). It records the status information.

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STATUS	--	POWER	VOLT	$\overline{TO}$	$\overline{PD}$	Z	DC	C

- Bit4 ($\overline{TO}$): Timer overflow flag bit
- Bit3 ($\overline{PD}$): Power down flag bit

$\overline{TO}$	$\overline{PD}$	Description
0	0	WDT timer overflow (4'key reset) from sleep mode
0	1	WDT timer overflow (4'key reset) from normal mode
1	0	Input a 'low" at RESETB from sleep mode Sleep instruction
1	1	Power on reset CLRWDT instruction
Unchanged	Unchanged	Input a "low" at RESETB from normal mode

- Bit2 (Z): zero flag bit

  0: the result of a logic operation is not zero

  1: the result of a logic operation is zero

- Bit1 (DC): Nibble Carry and Nibble $\overline{Borrow}$ flag bit

  ADD instruction:

  0: no carry

  1: a carry from the low nibble bits of the result occurred

  SUB instruction

  0: a borrow from the low nibble bits of the result occurred

  1: no borrow

- Bit0 (C): Carry and $\overline{Borrow}$ flag bit

  ADD instruction:

  0: no carry

  1: a carry occurred from the MSB

  SUB instruction

  0: a borrow occurred from the MSB

  1: no borrow

Bit	Symbol	Description	
6	POWER	POWER: POWER control 1: Don't use 0: normal mode	
5	VOLT	VOLT: I/O PAD voltage (read only) 1: 3V (MK9A35EP fixed) 0: Don't use	
4	$\overline{TO}$	Time out flag bit: 1: after power-on or by the CLRWDT or SLEEP instruction 0: Occur WDT time-overflow	
3	$\overline{PD}$	Power down flag bit: (Note2) 1: after power-on or by the CLRWDT instruction 0: execute SLEEP instruction	
2	Z	Zero bit: 1: the result of a logic operation is zero 0: the result of a logic operation is not zero	
1	DC	Nibble Carry and Nibble $\overline{Borrow}$ bit	
		ADD instruction	SUB instruction
		1: a carry from the low nibble bits of the result occurred 0: no carry	1: no borrow 0: a borrow from the low nibble bits of the result occurred
0	C	Carry and $\overline{Borrow}$ bit:	
		ADD instruction	SUB instruction
		1: a carry occurred from the MSB 0: no carry	1: no borrow (Note1) 0: a borrow occurred from the MSB

2.11 PCH & PCL:

PCH ($02h)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCH	--	--	--	--	A11	A10	A9	A8

PCL ($01h)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCL	A7	A6	A5	A4	A3	A2	A1	A0

The MK9A35FP has an 12-bits program counter (PC) that includes PCL (8-bits) and PCH (4-bits). PC is stored the routing of program. If user changes the value of PCL, then program will jump to the indicated location.

Ex1: PCH=01H, PCL=02H+10H=12H, the program will jump to PC=112H.

Ex2: PCH= 01H, PCL=F0H+30H=20H with carry 1, the program will jump to PC=220H but PCH still be 01H.

<Note>

(a) When execute IRET and IRETI, PCH data would not be updated

(b) When execute LGOTO, LCALL and RET, PCH would be updated .

(c) PCH would be updated after mathematic operation and PC[8] is changed.

2.12 Reset

There are 4 events will cause reset which is listed as below. The power-down event will cause MK9A35FP reset and the detected voltage is according to the bit7~bit6 in the CONFIG register. This condition is used to protect chip in deficient power environment. The last two cases are called warm reset. The different reset events will affect registers and RAM. The $\overline{TO}$ and $\overline{PD}$ bits can be used to determine the type of reset.

(1) Power-on reset. (Cold reset)

(2) Low voltage reset (LVR). (Cold reset)

(3) RESETB pin reset (input a negative pulse). (Warm reset)

(4) 4'S KEY reset. (Warm reset)

(5) WDT timer overflow reset. (Warm reset)

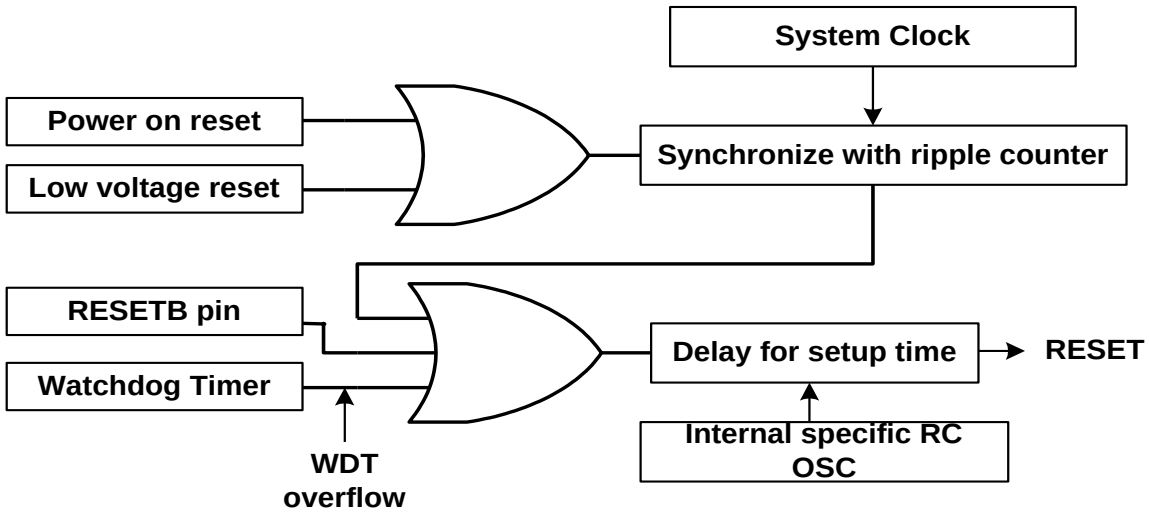


Fig.2.12.1 Reset Diagram

<Note>: the watchdog setup time is approximately 20ms that will has some tolerance due to power voltage, process and temperature variations. Setup time

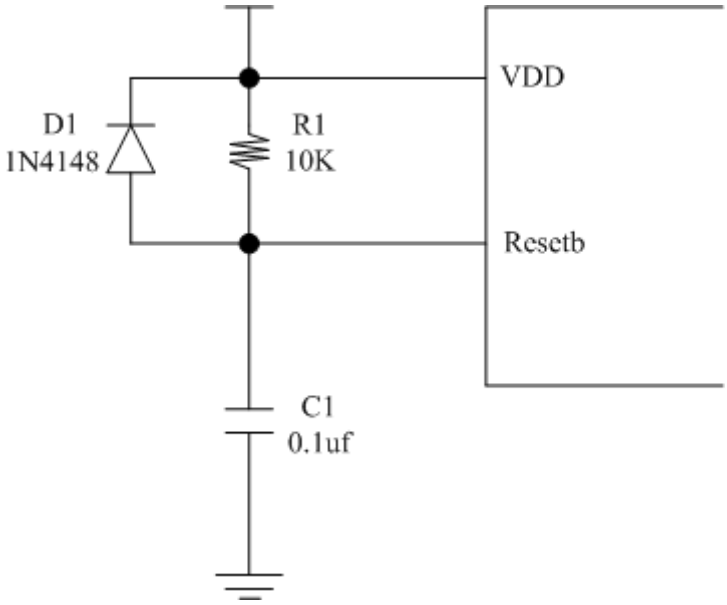


Fig.2.12.2 Reset Circuit

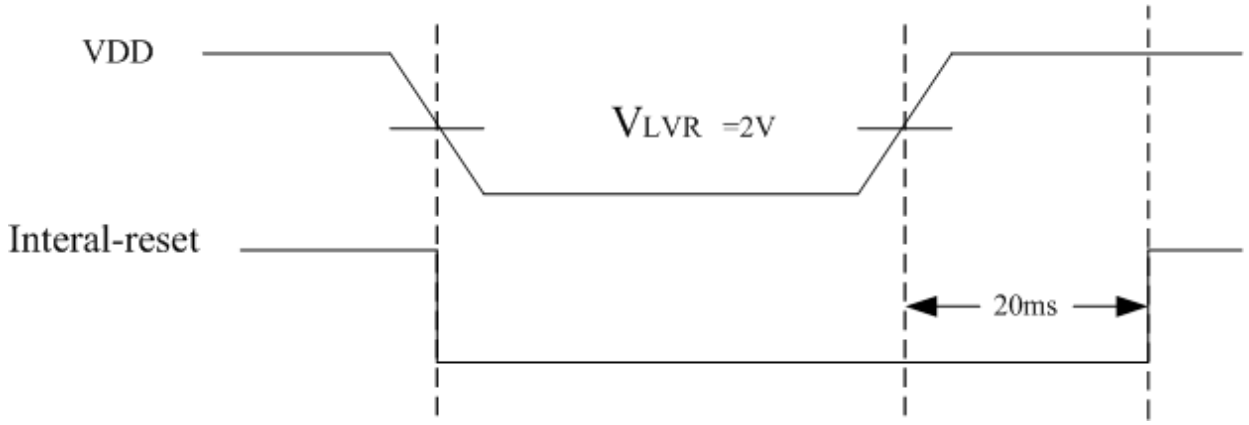


Fig.2.12.3 LVR ON

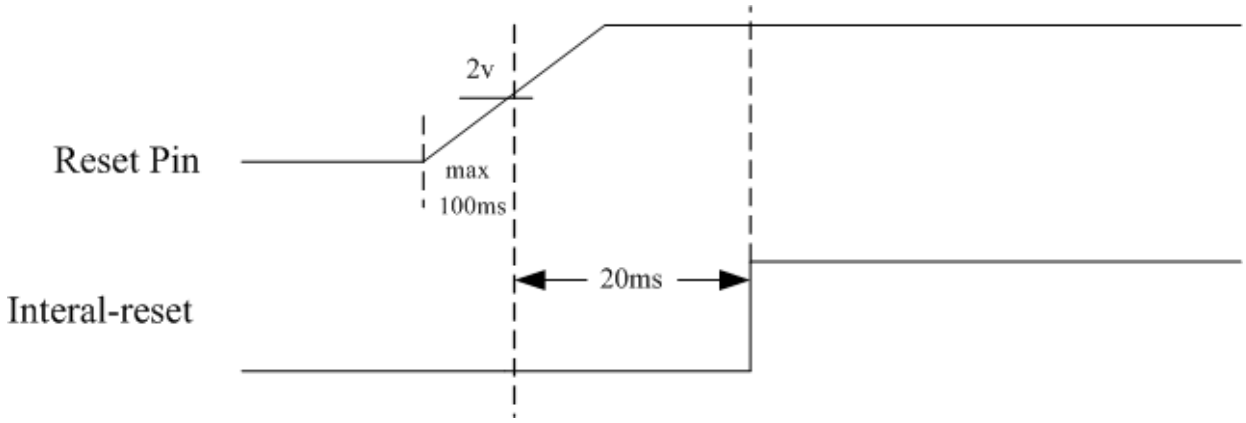


Fig.2.12.4 External Reset -- RESETB PIN

The default value during different reset condition

Address	Name	Cold Reset	Warm Reset
N/A	Accumulator	xxxx xxxx	PPPP PPPP
00H	INDF	0000 0000	0000 0000
01H	PCL	0000 0000	0000 0000
02H	PCH	- - - - 0000	- - - - 0000
03H	STATUS	0001 1000	0001 1000
04H	FSR	0000 0000	0000 0000
05H	PA_DIR	0111 1111	0111 1111
06H	PA_CTL	0000 0000	0000 0000
07H	WAKE_UP	0000 0000	0000 0000
08H	PA_PUD1	0000 0000	0000 0000
09H	PA_PUD2	0000 0000	0000 0000
0AH	PA_DAT	XXXX XXXX	PPPP PPPP
0BH	PC_CTL	0000 0000	0000 0000
0CH	PC_DIR	0001 1111	0001 1111
0DH	PC_PUD	0000 0000	0000 0000
0EH	PC_DAT	0000 0000	0000 0000
0FH	PD_DIR	1111 1111	1111 1111
10H	PD_PUD	0000 0000	0000 0000
11H	PD_CTL	0000 0000	0000 0000
12H	PD_DAT	0000 0000	0000 0000
13H	PAD_CTL1	0000 0000	0000 0000
14H	PAD_CTL2	0000 0000	0000 0000
15H	PAD_CTL3	0000 0000	0000 0000
17H	TM0_CTL	0000 0000	0000 0000
18H	TM0_LA	0000 0000	0000 0000
19H	TM0_CNT	0000 0000	0000 0000
1FH	TM2_CTL1	0000 0000	0000 0000
20H	TM2_CTL2	0000 0000	0000 0000
21H	TM2_LA	0000 0000	0000 0000
22H	TM2_CNT	0000 0000	0000 0000
23H	TM3_CTL1	0000 0000	0000 0000
24H	TM3_CTL2	0000 0000	0000 0000
25H	TM3_LA	0000 0000	0000 0000

26H	**TM3_CNT**	**0000 0000**	**0000 0000**
30H	**CPU_RESUME**	**0000 0000**	**0000 0000**
31H	**IRQM**	**0000 0000**	**0000 0000**
32H	**IRQF**	**0000 0000**	**0000 0000**
33H	**LBASDT**	**0101 0010**	**0101 0010**
34H	**STROBE**	**0000 0000**	**0000 0000**
35H	**LCD_CTL**	**0000 0000**	**0000 0000**
36H	**PH_CTL**	**0000 0000**	**0000 0000**
37H	**PH_OUT**	**PPPP PPPP**	**PPPP PPPP**
38H	**PH_OUT1**	**PPPP PPPP**	**PPPP PPPP**
39H	**TONE_CTL1**	**0000 0000**	**0000 0000**
3AH	**TONE_CTL2**	**0000 0000**	**0000 0000**
3BH	**WDT_CTL**	**1000 0111**	**1000 0111**
3DH	**TAB_BNK**	**0000 0000**	**0000 0000**
3EH	**SYS_CTL**	**0000 0010**	**0000 0010**

X: unknown; **?: value depends on condition ;**

P: previous data; **-:unimplemented and read as"0".**

3. Timer and Capture

3.1 16 bit Pre-divider

This 16 bit pre-divider can generate 2Hz timer interrupt which can provide an accurate 0.5sec timer base. By the way, some of this pre-divider timer would become time base of many other blocks, i.e. LCD driver, timer and capture. There are two registers which used to indicate each stage status of flip-flop of 16bit divider from PH which can be a time base for synchronization. These two registers can be read out.

PH_OUT ($37h) & PH_OUT1($38h): (R)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH_OUT	PH15	PH14	PH13	PH12	PH11	PH10	PH9	PH8
PH_OUT1	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH_OUT	1hz	2hz	4hz	8hz	16hz	32hz	64hz	128hz
PH_OUT1	256hz	512hz	1K	2K	4K	8K	16K	32K

3.2 Timer 0 (TM0)(up-counter)

Timer 0 has two functions in this chip, one is for general purpose 8 bit timer, the other is to be the time base of FREQ or Tone . TM0 has two buffers, TM0_LA and TM0_CNT. Before timer 0 starting to count, user should write counter value to TM0_LA. If WR_CNT (Bit 6 of TM0_CTL) is set to "1", then the data will automatically download to TM0_CNT (*Fig.3.2.2)*. This setting is need in the first time. After timer is counting and overflow is occurred, then it will generate interrupt and auto reload function will reload the TM0_LA data to TM0_CNT. The block is like below : (*Fig.3.2.1)*

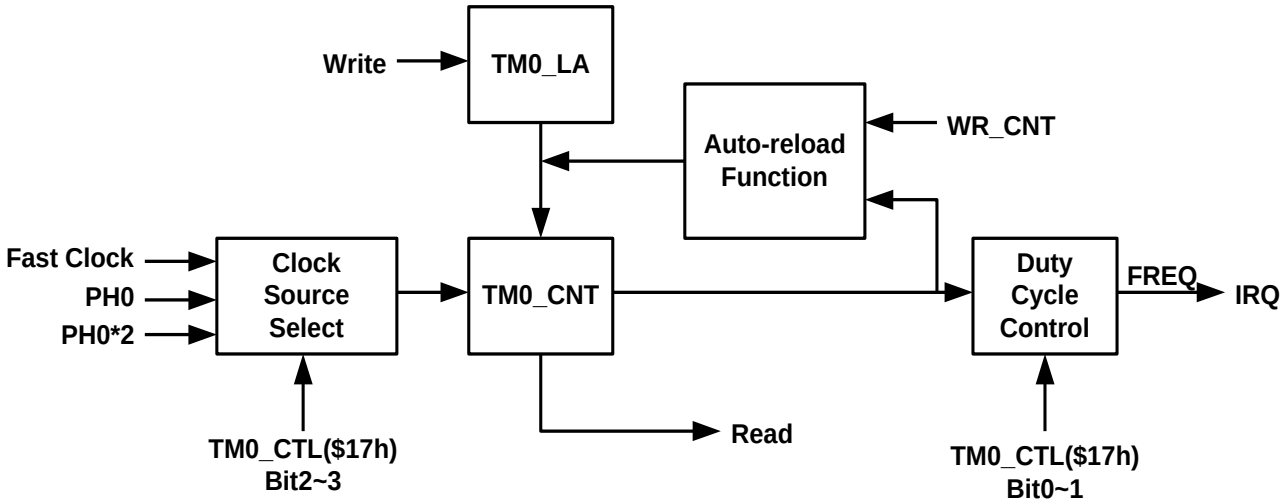


Fig.3.2.1 Timer 0 (TM0) Block Diagram

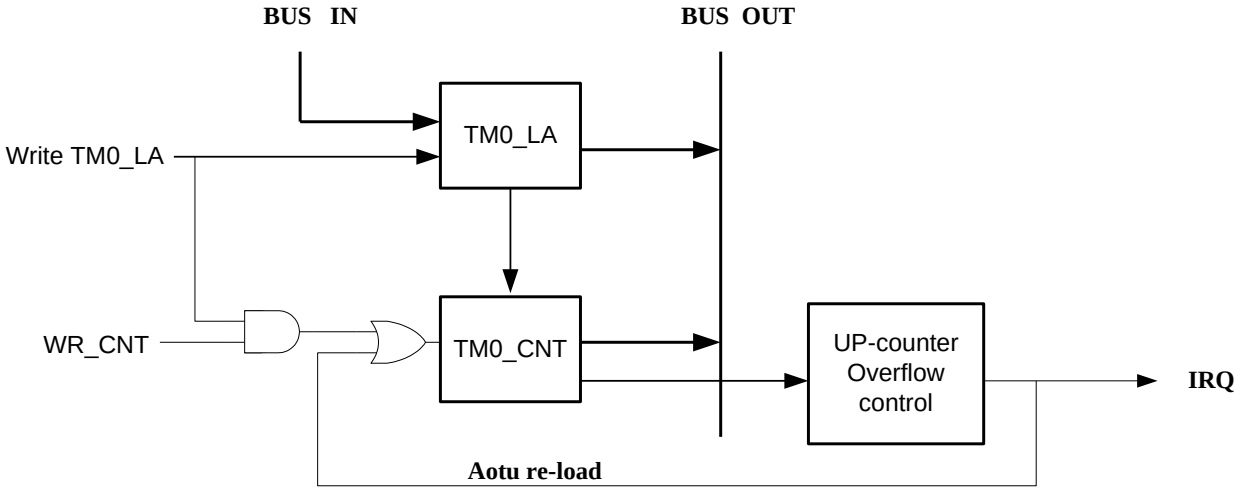


Fig.3.2.2 Timer 0 WR_CNT & auto-reload control

If TM0 is used as general purpose 8 bit timer, user can select the clock source by setting TM0_CTL($17h) register bit 2~3. The default value of duty cycle control block is (0,0) which means duty is 1:1. Because TM0 would be used to generate FREQ or Tone , the duty cycle may change to another value. Once user will switch among these functions, please take care these two bit data when use TM0 as general timer again.

3.3 FREQ and Tone

TM0 also can be used to generate FREQ and Tone. The block diagram is extended from TM0 block diagram. Please refer to below:

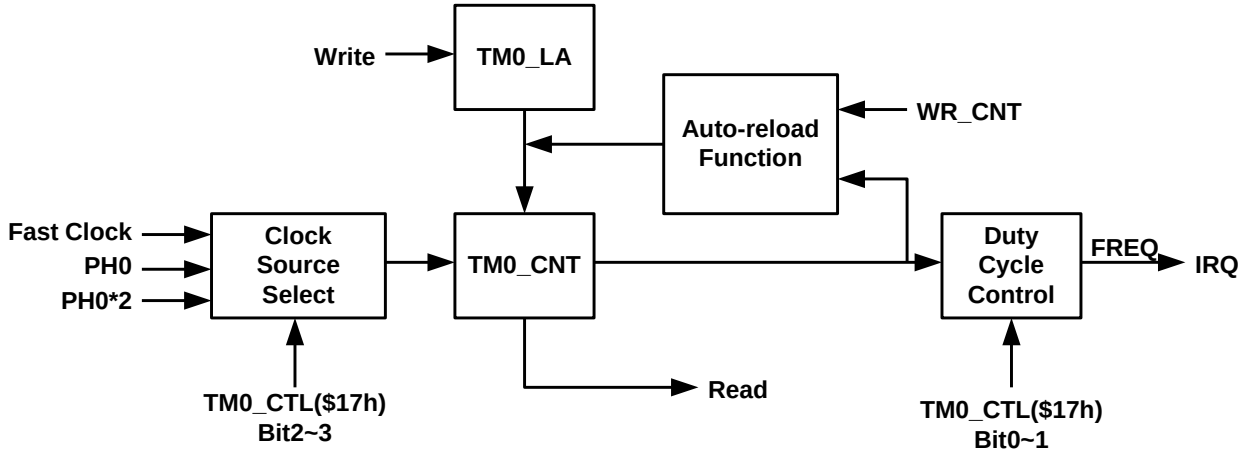


Fig.3.3.1 FREQ Block Diagram

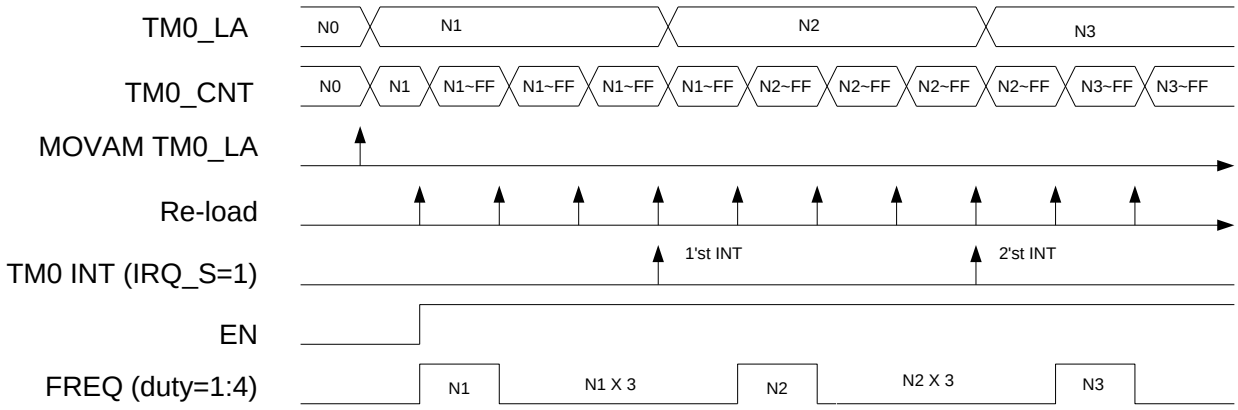


Fig.3.3.2 FREQ & INT waveform

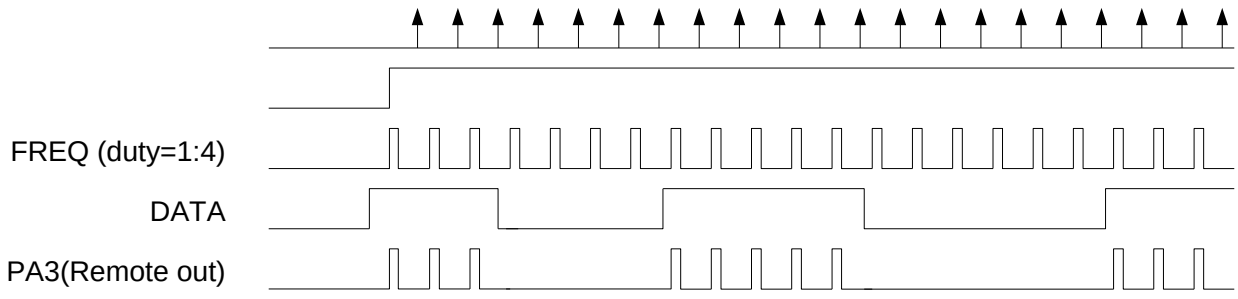


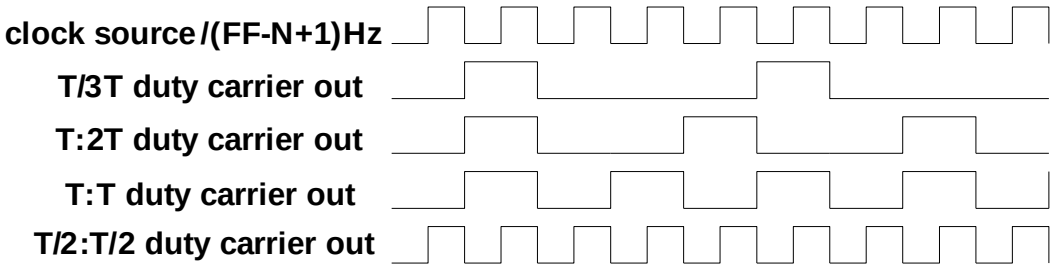
Fig.3.3.3 FREQ & INT waveform

The BZ output pin source can be FREQ or Tone by setting some register as below table. Because FREQ will also be the time base of some blocks, so it will always exist when TM0 is active.

TM0_CTL ($17h): TM0 Control

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM0_CTL	EN	WR_CNT	DATA	**IRQ_S**	SUR1	SUR0	DUTY1	DUTY0

Bit	Symbol	Description	
7	EN	TM0 enable /disable 0: Disable 1: Enable	
6	WR_CNT	TM0_CNT would be set through writing data to TM0_LA 0: Disable 1: Enable	
5	DATA	Remote mode , data output . (FREQ works as Carrier)	
4	**IRQ_S**	**Tm0 interrupt output** **0 : Tm0 overflow interrupt (RFC mode use)** **1 : FREQ cycle interrupt (Remote & FREQ use)**	
3~2	SUR1~0	SUR1~0 : TM0 clock source select	
		0 0	Fast clock
		0 1	PH0
		1 0	PH0 X 2
		1 1	PH6
1~0	DUTY1~0	DUTY1~0 : duty	
		0 0	1 : 1 H pulse:L pulse=T/2 : T/2
		0 1	1 : 2 H pulse:L pulse=T : T
		1 0	1 : 3 H pulse:L pulse=T : 2T
		1 1	1 : 4 H pulse:L pulse=T : 3T



<Note> If clock source/(FF-N+1) = (Odd number) Hz
The duty high = ((FF-N+1)+1)/2 The duty low = ((FF-N+1)-1)/2
Example : (FF-N+1)=3, H=2, L=1

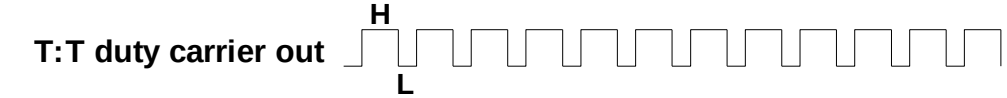


Fig.3.3.4 Timing Chart of Duty Setting

TM0_LA ($18h): TM0 data (R/W)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM0_LA	D7	D6	D5	D4	D3	D2	D1	D0

- Bit7~0: Timer 0 latch data (Data =/= FFh)

TM0_CNT($19h): TM0 counter (R) (up counter)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM0_CNT	D7	D6	D5	D4	D3	D2	D1	D0

- Bit7~0: Timer 0 counter data

<Note> 1. TM0 is up-count timer

2. Has auto reload function

TONE_CTL1 ($39h): (W)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TONE_CTL1	EN	PH15E	PH14E	PH13E	PH12E	PH11E	PAT1	INV12

- Bit7: Tone enable signal
  0 : Tone disable
  1 : Tone enable
- Bit6: PH15 enable/disable
  0: Disable
  1: Enable
- Bit5: PH14 enable/disable
  0: Disable
  1: Enable
- Bit4: PH13 enable/disable
  0: Disable
  1: Enable
- Bit3: PH12 enable/disable
  0: Disable
  1: Enable
- Bit2: PH11 enable/disable
  0: Disable
  1: Enable
- Bit1: (PH14 and PH13) enable/disable
  0: Disable
  1: Enable
- Bit0: Delay 1/16sec enable/disable
  0: Disable
  1: Enable

TONE_CTL2 ($3Ah): (W)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TONE_CTL2						CRY2	CRY1	CRY0

- Bit2-0: carrier select signal

  000 : FREQOUT carrier

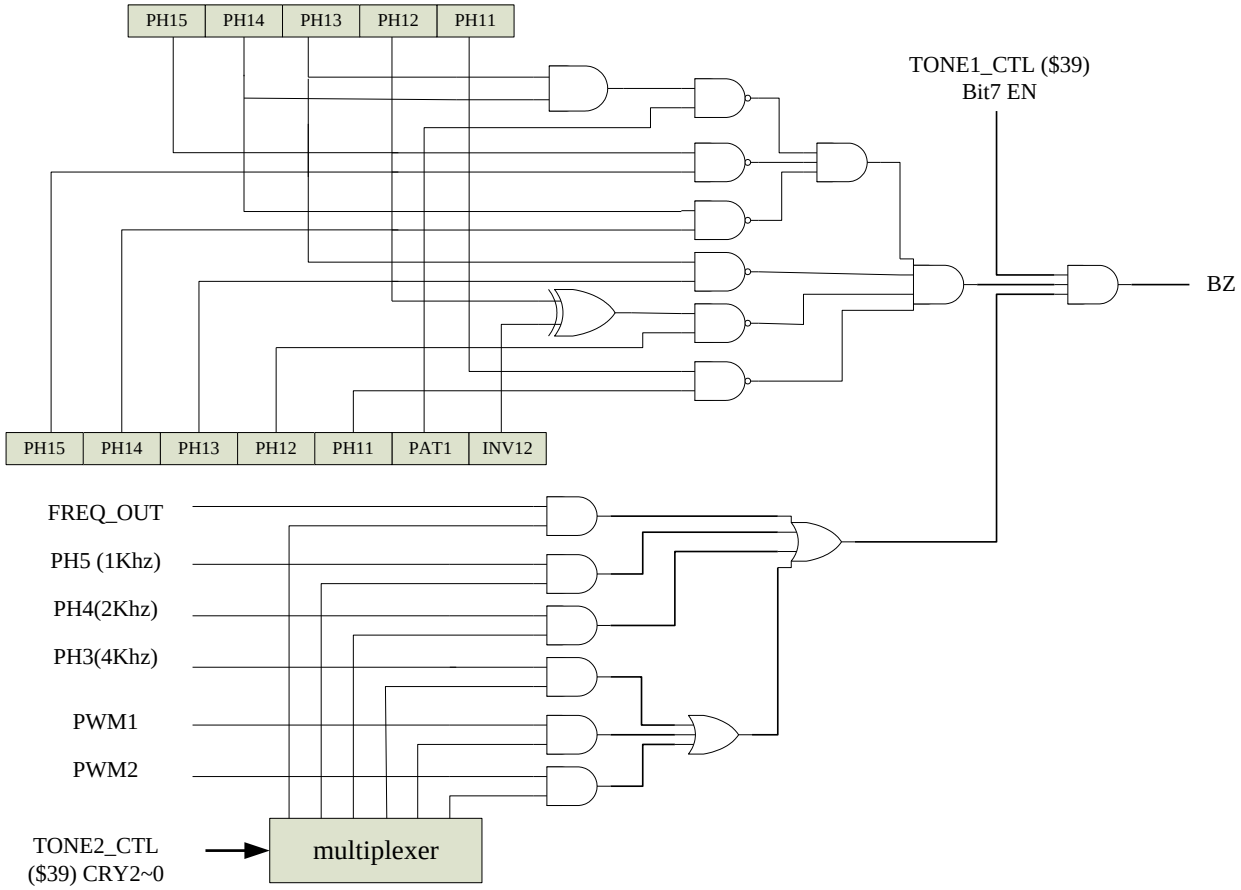
  001 : 1Khz carrier

  010 : 2Khz carrier

  011 : 4Khz carrier

  100 : PWM1 (TM2 pwm output)

  101 : PWM2 (TM3 pwm output)



Timing Chart of Duty Setting

3.4 Timer 2&3 (TM2 & TM3)(up-counter)

This two timers are multifunctional which can be set as independently 8 bit timer. The second operation mode is used to be event counters of capture to count external event from CAPT1A and CAPT1B pins. They can be used as two 8 bit counters independently . All the functions are setting by below registers and the block diagram are as below:

TM2_CTL1($1Fh)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM2_CTL1	EN	WR_CNT	**BIT**	MOD1	MOD0	EDGE	SUR1	SUR0

Bit	Symbol	Description			
7	EN	TM2 enable /disable 0: Disable 1: Enable			
6	WR_CNT	TM2_CNT would be set through writing data to TM2_LA (Timer ,capture ,pwm & RFC mode) 0: Disable 1: Enable			
5	BIT	BIT : 16-bit/8-bit control			
		0	8-bit mode.		
		1	16-bit mode , TM2 (high byte)+TM3 (low byte).		
4~3	MOD1~0	MOD1~0: TM2 operation mode selected			
		0 0	Timer mode		
		0 1	Capture mode		
		1 0	RFC mode		
		1 1	PWM mode		
2	EDGE	Capture signal edge control bit 1:increment when H→L transition on external clock 0:increment when L→H transition on external clock			
1~0	SUR1~0	Clock Source **(8-bit pwm mode ,PWM duty clock source comes from PH0X2)**			
				PWM mod,BIT=0	PWM mod,BIT=1
			TIMER,CAPTURE	**Period**	**Period**
		0 0	FCLK (Fast clock)	PH3	FCLK (Fast clock)

		0 1	PH0 X 2	PH4	PH0 X 2
		1 0	PH4	PH5	PH4
		1 1	PH_CLK	PH_CLK	PH_CLK

TM2_CTL2($20h):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM2_CTL2	ENC	CLR_CNT			CAPIN0/ RFC_T0	INT_S	PWM_OS	OV

Bit	Symbol	Description		
7	ENC	**Capture & RFC mode**: counter auto clear (When overflow) 0: Auto clear counter (Hardware mode) 1: Clear counter by software.		
6	CLR_CNT	**Capture & RFC mode**: Clear counter (When ENC=1 and work in capture mode or RFC mode) 0: No clear 1: Clear counter and auto clear CLR_CNT		
3	CAPIN0/ RFC_T0	1. Signal Source Select (Work in capture mode only) 2. IRQ source select (Work in RFC mode only)		
		mode	Capture mode	RFC mode
		0	CAPT1A input	TMR0 IRQ
		1	CAPT1B input	PH IRQ
2	INT_S	Signal Source Select (Work in RFC or Capture mode)		
		INT_S	Capture mode	RFC mode
		0	CAPTURE IRQ	No IRQ
		1	RFC overflow IRQ	RFC overflow IRQ
1	PWM_OS	PWM_OS: Output state of PWM select bit.		
		0	The initial output state is H, this will change to L when timer overflow.	
		1	The initial output state is L, this will change to H when timer overflow.	
0	OV	Overflow bit (capture & RFC mode, user should clear this bit after reading) 0: No overflow 1: Overflow		

TM2_LA ($21h): TM2 data (R/W)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM2_LA	D7	D6	D5	D4	D3	D2	D1	D0

TM2_CNT($22h): TM2 counter (R/W) (up counter)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM2_CNT	D7	D6	D5	D4	D3	D2	D1	D0

TM3_CTL1($23h)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM3_CTL1	EN	WR_CNT	--	MOD1	MOD0	EDGE	SUR1	SUR0

<table>
<tr><th>Bit</th><th>Symbol</th><th colspan="4">Description</th></tr>
<tr><td>7</td><td>EN</td><td colspan="4">TM3 enable /disable
0: Disable
1: Enable</td></tr>
<tr><td>6</td><td>WR_CNT</td><td colspan="4">TM3_CNT would be set through writing data to TM3_LA
(Timer ,capture ,pwm & RFC mode)
0: Disable
1: Enable</td></tr>
<tr><td rowspan="5">4~3</td><td rowspan="5">MOD1~0</td><td colspan="4">MOD1~0: TM3 operation mode selected</td></tr>
<tr><td>0 0</td><td colspan="3">Timer mode</td></tr>
<tr><td>0 1</td><td colspan="3">Capture mode</td></tr>
<tr><td>1 0</td><td colspan="3">RFC mode</td></tr>
<tr><td>1 1</td><td colspan="3">PWM mode (TM3 comes from PH0X2 input)</td></tr>
<tr><td>2</td><td>EDGE</td><td colspan="4">Capture signal edge control bit
1:increment when H→L transition on external clock
0:increment when L→H transition on external clock</td></tr>
<tr><td rowspan="5">1~0</td><td rowspan="5">SUR1~0</td><td colspan="4">Clock Source
(8-bit pwm mode ,PWM duty clock source comes from PH0X2)</td></tr>
<tr><td></td><td></td><td>PWM mod,BIT=0</td><td>PWM mod,BIT=1</td></tr>
<tr><td></td><td>TIMER,CAPTURE</td><td>Period</td><td>Duty</td></tr>
<tr><td>0 0</td><td>FCLK (Fast clock)</td><td>PH3</td><td>FCLK (Fast clock)</td></tr>
<tr><td>0 1</td><td>PH0 X 2</td><td>PH4</td><td>PH0 X 2</td></tr>
</table>

		1 0	PH4	PH5	PH4
		1 1	PH_CLK	PH7	PH_CLK

TM3_CTL2($24h):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM3_CTL2	ENC	CLR_CNT	--	--	CAPIN/ RFC_T	INT_S	PWM_OS	OV

Bit	Symbol	Description
7	ENC	Capture & RFC mode: counter auto clear (When overflow) 0: Auto clear counter (Hardware mode) 1: Clear counter by software.
6	CLR_CNT	Capture & RFC mode: Clear counter (When ENC=1 and work in capture mode or RFC mode) 0: No clear 1: Clear counter and auto clear CLR_CNT
3	CAPIN0/ RFC_T0	3. Signal Source Select (Work in capture mode only) 4. IRQ source select (Work in RFC mode only)
		mode / Capture mode / RFC mode
		0 / CAPT1A input / TMR0 IRQ
		1 / CAPT1B input / PH IRQ
2	INT_S	Signal Source Select (Work in capture or RFC mode)
		INT_S / Capture mode / RFC mode
		0 / CAPTURE IRQ / No IRQ
		1 / RFC overflow IRQ / RFC overflow IRQ
1	PWM_OS	PWM_OS: Output state of PWM select bit.
		0 / The initial output state is L, this will change to H when timer overflow.
		1 / The initial output state is H, this will change to L when timer overflow.
0	OV	Overflow bit (**capture & RFC** mode only, user should clear this bit after reading) 0: No overflow 1: Overflow

TM3_LA ($25h): TM3 data (R/W)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM3_LA	D7	D6	D5	D4	D3	D2	D1	D0

TM3_CNT($26h): TM3 counter (R/W) (up counter)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM3_CNT	D7	D6	D5	D4	D3	D2	D1	D0

3.5 Watchdog Timer (WDT)

WDT is a timer to prevent software from malfunction or jumping to an unknown location with unpredictable result. The source clock of WDT is slow clock. User should enable or disable watchdog timer by configuration register bit 5 (WDTE) at first.

WDT CTL ($3Bh):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDT_CTL	WDTEN	--	--	--	--	PRE 2	PRE 1	PRE0

- Bit7 (WDTEN): Watchdog timer enable/disable bit

  0: WDT disable.

  1: WDT enable.

<Note> Bit6~5 (TEST1/TEST0) are reserved bit for testing

- Bit2~0 (PRE2~0): WDT prescaler assignment bit.

Bit2	Bit1	Bit0	WDT Prescaler rate
PRE2	PRE1	PRE0	
0	0	0	Twdt
0	0	1	Twdt X 2
0	1	0	Twdt X 4
0	1	1	Twdt X 8
1	0	0	Twdt X 16
1	0	1	Twdt X 32
1	1	0	Twdt X 64
1	1	1	Twdt X128 (2'S key reset mode)

CONFIG		OSC Type	Twdt
SOSC1	SOSC0		
0	0	LP (low speed)	Twdt = Tsystem clock X 512
0	1	NO	Twdt = 15.6 mS
1	1	Internal RC	Twdt = 15.6 mS

Table 3.5.1 The relation between slow clock type and WDT

4. I/O Port and Other Control Function

I/O port

There are 3 I/O port groups PA, PC and PD to input or output data, each port has different definition and most of them share the pin with other functions. Port A (PA) is bi-direction I/O port which has pull-up, pull-down, open-drain and pin change wake up functions by setting. Port C (PC) and Port D (PD) has pull-down & pmos open-drain .

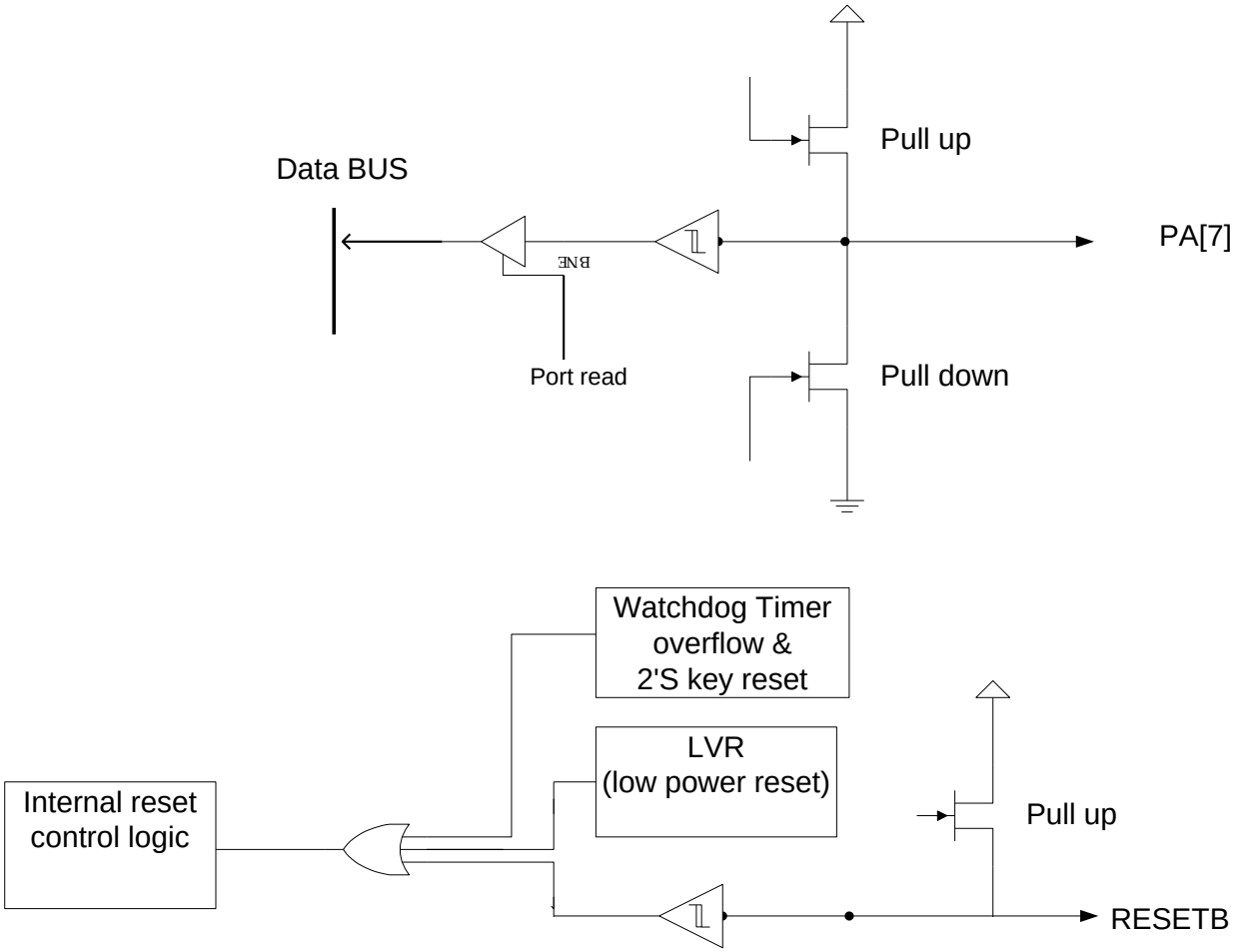


Fig.4.1.1-1 RESETB (PA7) STRUCTURE

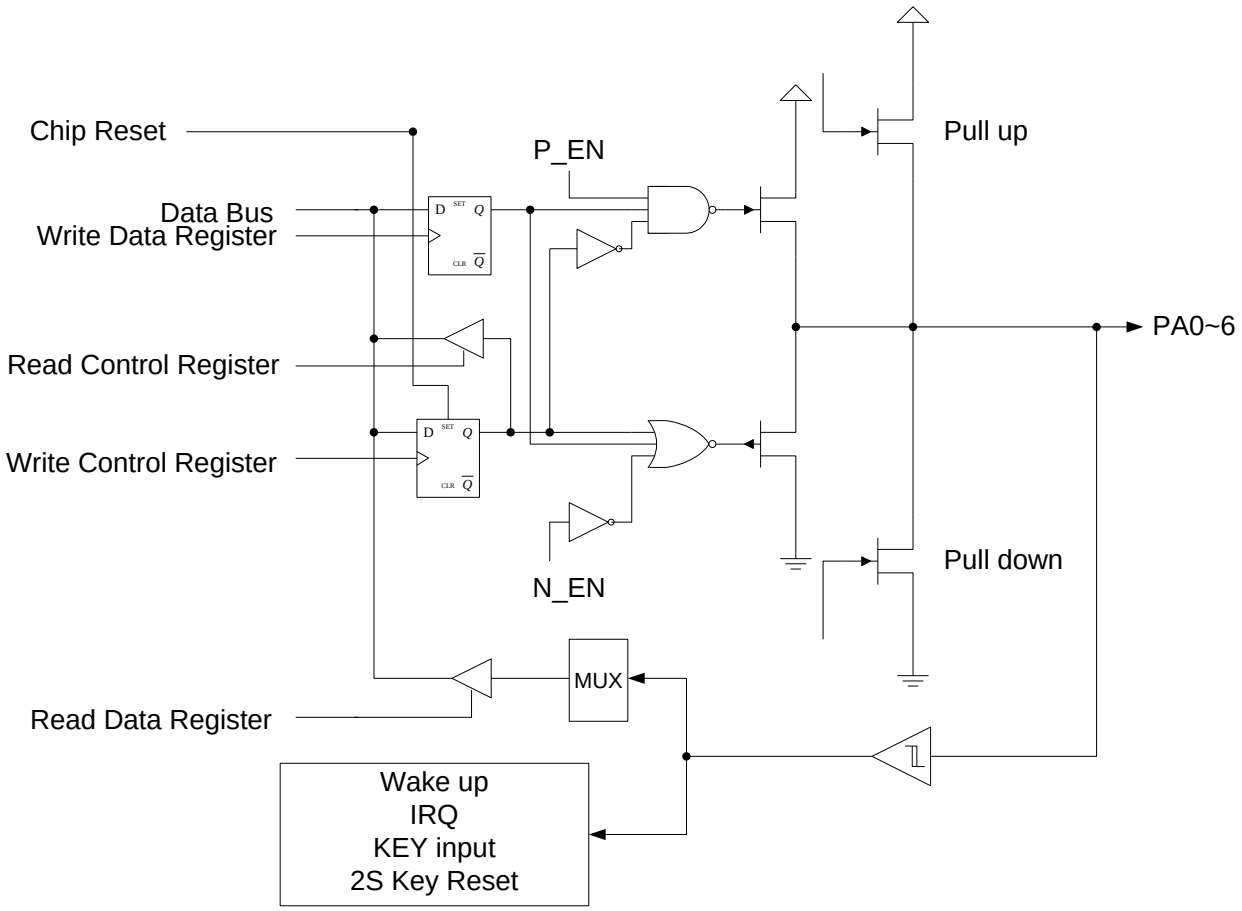


Fig.4.1.1-2 PORT A STRUCTURE

4.1.1. Port A (PA)

Port A is the only one bidirectional I/O port in this chip. It has pull up, pull down, open-drain and pin wake up function. It also can replace RESET pin to act as power on reset if user set configuration bit. There are 6 registers to set the 8 I/O ports which are PA_DIR, PA_DAT, WAKE_UP, PA_PUD1 and PA_PUD2. The registers are defined as below:

PA_DIR ($05h):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PA_DIR	--	CA6	CA5	CA4	CA3	CA2	CA1	CA0

- Bit6~0 (CA6~0): Set PA as input port or output port. (PA[7] only can be input port only)
  0: Output port
  1: Input port

WAKE_UP ($07h)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WAKE_UP	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0

- Bit7~0 (PA7~0): Pin PA7~0 pin change wake-up control bits.

  0: Wake up disable

  1: Wake up enable (Only active when PA was set as input at PAD_CTL1 ($13h)

CAn (PA_DIR)	ENn (WAKE_UP)	KI (Pin-change wake-up function)
1	1	ON
X	0	OFF
0	1	OFF

PA_PUD1 ($08h) & PA_PUD2 ($09h)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PA_PUD1	A3-2	A3-1	A2-2	A2-1	A1-2	A1-1	A0-2	A0-1
PA_PUD2	A7-2	A7-1	A6-2	A6-1	A5-2	A5-1	A4-2	A4-1

- When set PA as I/O port (PAD_CTL2) and direction is input (PA_DIR), then

  An-1=1 -> PAn pull down

  An-2=1 -> PAn pull up

- When set PA as I/O port (PAD_CTL2) and direction is output (PA_DIR), then

  An-1=1 -> PMOS open drain on

  An-2=1 -> NMOS open drain on

These two registers are used to set PA to have pull-up or pull-down resistor. But this only active with PAD_CTL2 was set as I/O port and PA_DIR was set as input. The relation between them are as below table.

KIn/PAn (PAD_CTL2)	CAn (PA_DIR)	An-2	An-1	PULL-UP	PULL-DOWN	PMOS OPEN-DRAIN	NMOS OPEN-DRAIN	Description PAn (n=0~6)
I/O	1	0	0	OFF	OFF	OFF	OFF	PAn is input port
I/O	1	0	1	OFF	**ON**	OFF	OFF	PAn is input port
I/O	1	1	X	**ON**	OFF	OFF	OFF	PAn is input port
I/O	0	0	0	OFF	OFF	ON	ON	PAn is normal output
I/O	0	0	1	OFF	OFF	ON	OFF	PAn is nmos open -drain output port
I/O	0	1	X	OFF	OFF	OFF	ON	PAn is pmos open -drain output port

<Note> (1) PA[7] is shared the pin with RESETB which can be used as input port only. So, there is only pull up/down function can be set as below table.

I/O	A7-2	A7-1	PULL-DOWN	PMOS OPEN-DRAIN	NMOS OPEN-DRAIN	PA7
PA7	0	0	OFF	OFF	OFF	PA7 is input port
PA7	0	1	**ON**	OFF	OFF	PA7 is input port
PA7	1	X	OFF	OFF	OFF	Don't use

PA _DAT($0Ah):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PA_DAT	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0

- Bit6~0 (PA6~0): PA input or output data bits.
- Bit7: Input data only.

<Note> PA[5]~PA[7] share the pin with OSCOUT, OSCIN and RESETB. If user want to use these pins as PA, then the Configuration bit 3~2 (FOSC1 and FOSC0) must set to (0,1). And bit 8 (RST_DEF) must set to 0 as normal input port.

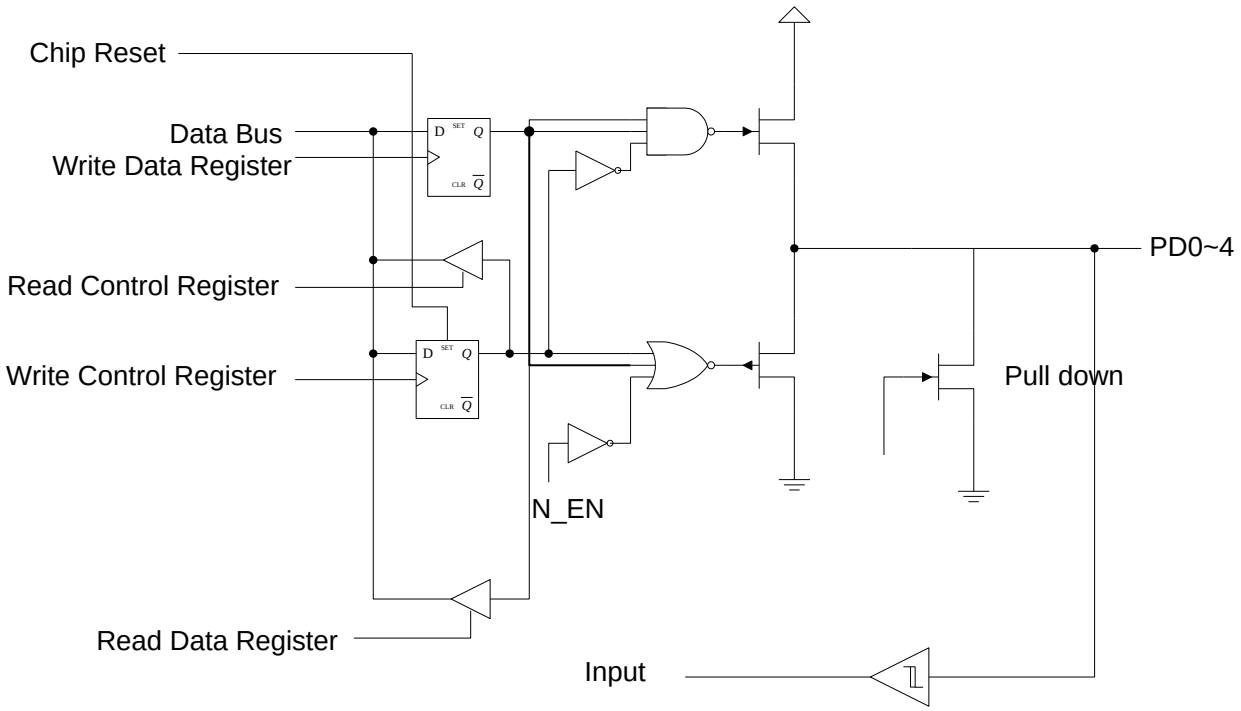


Fig.4.1.2 PORT C STRUCTURE

4.1.2 Port C (PC)

There are 4 registers to set the attribute of Port C which are PC_CTL,PC_DIR,PC_PUD and PC_DAT. Port C is bidirectional I/O port when it was used as I/O port.

PC_CTL ($0Bh): (R/W) (default =00000000b)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PC_CTL	--	--	--	--	--	--	KI1/IO1	KI0/IO0

- Bit1~0 (KI1/IO1): PC1~0 work as KI or I/O input mode (input only)
  0: IO input mode
  1: KEY input

PORT	KIn/ IOn	PAD_CTL8	STROBE Bit6 EN	PC_DIR	PC_PUD	condition	PULL-DOWN	OUT	Description PDn (n=0~6)
PC0	KI	–	1	1	X	1.COM7 is off 2.PC0 works as I/O input	ON	OFF	PC0 is avail key input
			0				OFF		Key function is off. No power consumption.
PC1	KI	–	1	1	X	1.COM6 is off 2.PC1 works as I/O input	ON	OFF	PC1 is avail key input
			0				OFF		Key function is off. No power consumption.

PC_DIR ($0Ch): (R/W) (default =00000000b)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PC_DIR	--	--	--	DC4	DC3	DC2	DC1	DC0

- Bit4~0 (DC4~0): Set PC as input port or output port.
  0: Output port
  1: Input port

PC_PUD ($0Dh) : (R/W) (default =00000000b)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PC_PUD	--	--	--	CD4	CD3	CD2	CD1	CD0

<Note> When these shared pins are set as PC, there are PMOS open drain or NMOS open drain can be selected. The setting method is as below table:

DDn	Dn-1	PULL-	PMOS	Description

(PC_DIR)		DOWN	OPEN-DRAIN	PCn (n=0~4)
1	0	OFF	OFF	PCn is input port
1	1	**ON**	OFF	PCn is input port
0	0	ON	ON	PCn is normal output
0	1	OFF	ON	PCn is pmos open drain output port

PC _DAT($0Eh): (R/W) (default =00000000b)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PC_DAT	--	--	--	PC4	PC3	PC2	PC1	PC0

- Bit4~0 (PC4~0): PC input data bits.

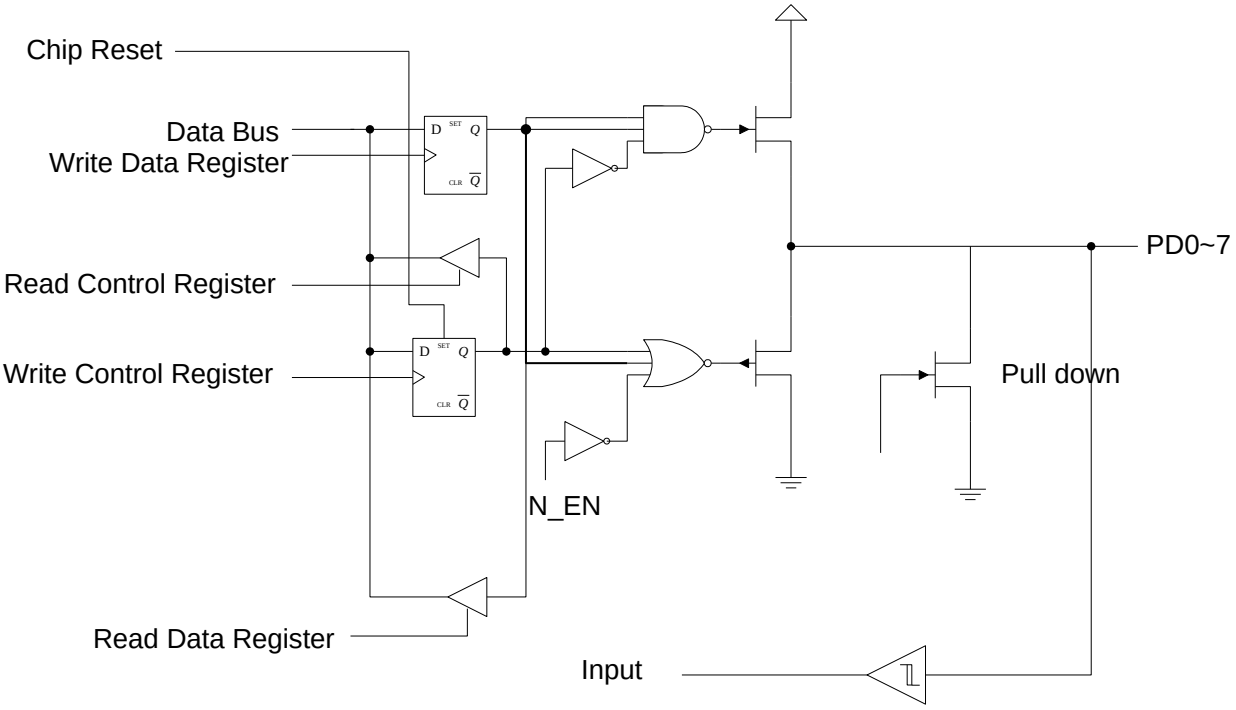


Fig.4.1.3 PORT D STRUCTURE

4.1.3 Port D (PD)

There are 4 registers to set the attribute of Port D which are PD_DIR, PD_PUD,PD_CTL and PD_DAT. Port D is bidirectional I/O port when it was used as I/O port.

PD_DIR ($0Fh): (R/W) (default =11111111b)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PD_DIR	DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0

- Bit7~0 (DD7~0): Set PD as input port or output port.

0: Output port

1: Input port

PD_PUD ($10h) : (R/W) (default =00000000b)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PD_PUD	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0

<Note> When these shared pins are set as PD, there are PMOS open drain or NMOS open drain can be selected. The setting method is as below table:

DDn (PD_DIR)	Dn-1	PULL-DOWN	PMOS OPEN-DRAIN	Description PDn (n=0~5)
1	0	OFF	OFF	PDn is input port
1	1	**ON**	OFF	PDn is input port
0	0	ON	ON	PDn is normal output
0	1	OFF	ON	PDn is pmos open drain output port

PD_CTL ($11h): (R/W) (default =00000000b)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PD_CTL	KI7/IO7--	KI6/IO6--	KI5/IO5--	KI4/IO4	KI3/IO3	--KI2/IO2	KI1/IO1--	-KI0/IO0-

- Bit4~3 (DC4~3): PD work as KEY or I/O input mode (input only)

  0: I/O input port

  1: Key Input port

PORT	KIn/ IOn	PAD_CTL1 BITn	STROBE Bit6 EN	PD_DIR	PD_PUD	condition	PULL-DOWN	OUT	Description PDn (n=0~6)
PD0	KI	0 SEG OFF	1	1	X	--	ON	OFF	PD0 is avail key input
			0				OFF		Key function is off. No power consumption.
PD1	KI	0 SEG OFF	1	1	X	--	ON	OFF	PD1 is avail key input
			0				OFF		Key function is off. No power consumption.
PD2	KI	0 SEG OFF	1	1	X	--	ON	OFF	PD2 is avail key input
			0				OFF		Key function is off. No power consumption.
PD3	KI	0 SEG OFF	1	1	X	--	ON	OFF	PD3 is avail key input
			0				OFF		Key function is off. No power consumption.
PD4	KI	0 SEG OFF	1	1	X	--	ON	OFF	PD4 is avail key input
			0				OFF		Key function is off. No power consumption.
PD5	KI	0 SEG OFF	1	1	X	--	ON	OFF	PD5 is avail data input
			0				OFF		Key function is off. No power consumption.
PD6	KI	0 SEG OFF	1	1	X	PH_CTL Bit5 EL_P=0	ON	OFF	PD6 is avail data input
			0				OFF		Key function is off. No power consumption.
PD7	KI	0 SEG OFF	1	1	X	PH_CTL Bit5 EL_P=0	ON	OFF	PD7 is avail data input
			0				OFF		Key function is off. No power consumption.

PD _DAT($12h):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PD_DAT	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

- Bit7~0 (PD7~0): PD output data bits.

Define Shared Pin

PAD_CTL1 ($13h): (R/W) (default =00000000b)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

PAD_CTL1	SEG27/ PD[7]	SEG26 /PD[6]	SEG25/ PD[5]	SEG24 /PD[4]	SEG23/ PD[3]	SEG22/ PD[2]	SEG21/ PD[1]	SG20/ PD[0]

<Note> This register is used to set the shared pin function which can be set as below table.

Bit	Bitn=1	Bitn=0
0	SEG20	PD[0]
1	SEG21	PD[1]
2	SEG22	PD[2]
3	SEG23	PD[3]
4	SEG24	PD[4]
5	SEG25	PD[5]
6	SEG26	PD[6]/ELP
7	SEG27	PD[7]/ELC

Bit \value	11	10	01	00
(PH_CTL.EL_P),B6	Don"t use	ELP	SEG26	PD6
(PH_CTL.EL_P),B7	Don"t use	ELC	SEG27	PD7

PAD_CTL2 ($14h): (R/W) (default =00000000b)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PAD_CTL2	--	C6	C5	C4	C3	C2	C1	C0

<Note> This register is used to set the shared pin function which can be set as below table.

Bit \value	0	1
C0	PA0	CAP
C1	PA1	REF
C2	PA2	SEN0
C3	PA4	BZ
C6	PA5	BZM

Bit \value	11	10	01	00
C5-C4	PWM1	SEN1	REM	PA3+CAPT1A

PAD_CTL3 ($15h): (R/W) (default =00000000b)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PAD_CTL3	EDGE	--	--	--	--	SEN1_ON	SEN0_ON	REF_ON

<Note> This register is used to set the shared pin function which can be set as below table.

- Bit7 (EDGE): PD[5] pin-interrupt control
  0: Rising edge
  1: Falling edge
- Bit2 (SEN1_ON): Set SEN1 pin output control (RFC mode only)
  0: Input disable
  1: input enable
- Bit1 (SEN0_ON): Set SEN0 pin output control (RFC mode only)
  0: Input disable
  1: input enable
- Bit0 (REF_ON): Set REF pin output control (RFC mode only)
  0: Input disable
  1: input enable

Key Strobe Function

The key scanning function use partial of segment frame frequency cycle to output scanning timing. This function would be limited to normal mode only

The register bits are defined as below:

STROBE($34h): Strobe Control (R/W) (default =000x0000b)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STROBE	FRAME	EN	KOAEN	KOEN	KO3	KO2	KO1	KO0

MODE/FUNCTION	SEG1~16	PORT PD[0~7] & PC[0:1]	PORT PA[0~6]
EN	X	Pull down enable	Can"t connect to SEGn
KOAEN	SEG1~16 : Hi output	X	X
KOEN	SEGn : Hi output Others : Floating	X	X

- Bit7 (FRAME): FRAME (read only)
  - 0: key input data is invalid
  - 1: key input data is valid
- Bit6 (EN): Key function enable
  - 0: disable
  - 1: enable
- Bit5 (KOAEN): Segment out control
  - 0: SEG1~16 : LCD output
  - 1: SEG1~16 : Hi output
- Bit4 (KOEN): Segment out control
  - 0: SEG1~16 : LCD output
  - 1: SEGn : Hi output ,others : floating output
- Bit3~0(KO3~0): Select which strobe pin to output signal as the table.

Bit3~0	KS1	KS2	KS3	KS4	KS5	KS6	KS7	KS8	KS9	KS10	KS11	KS12	KS13	KS14	KS15	KS16
0000	HI	f	f	f	f	f	f	f	f	f	f	f	f	f	f	f
0001	f	HI	f	f	f	f	f	f	f	f	f	f	f	f	f	f
0010	f	f	HI	f	f	f	f	f	f	f	f	f	f	f	f	f
0011	f	f	f	HI	f	f	f	f	f	f	f	f	f	f	f	f
0100	f	f	f	f	HI	f	f	f	f	f	f	f	f	f	f	f
0101	f	f	f	f	f	HI	f	f	f	f	f	f	f	f	f	f
0110	f	f	f	f	f	f	HI	f	f	f	f	f	f	f	f	f
0111	f	f	f	f	f	f	f	HI	f	f	f	f	f	f	f	f
1000	f	f	f	f	f	f	f	f	HI	f	f	f	f	f	f	f
1001	f	f	f	f	f	f	f	f	f	HI	f	f	f	f	f	f
1010	f	f	f	f	f	f	f	f	f	f	HI	f	f	f	f	f
1011	f	f	f	f	f	f	f	f	f	f	f	HI	f	f	f	f
1100	f	f	f	f	f	f	f	f	f	f	f	f	HI	f	f	f
1101	f	f	f	f	f	f	f	f	f	f	f	f	f	HI	f	f
1110	f	f	f	f	f	f	f	f	f	f	f	f	f	f	HI	f
1111	f	f	f	f	f	f	f	f	f	f	f	f	f	f	f	HI

PS. f – floating

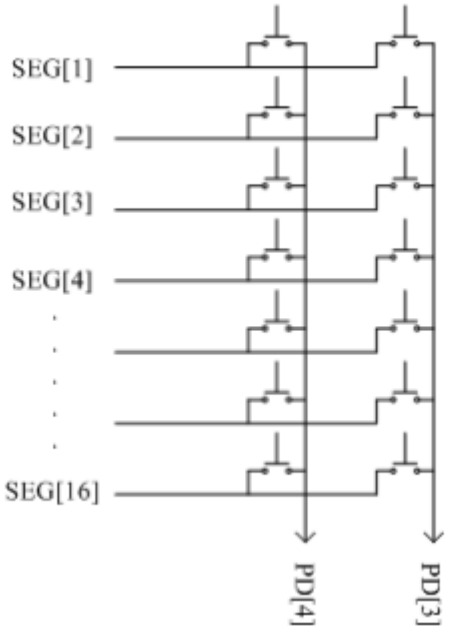


Fig.4.3.1 Software mode (PD[4:3]-input, SEG)-output)

Interrupt & halt release

The MK9A35FP provides 7 interrupt event. IRQM and IRQF registers are used to control or declare request state of all interrupts. The external interrupt is triggered by a high to low transition signal of PA0~7 and the related interrupt request flag (PAF; bit6 of IRQF) will be set. IRQM is used to enable/disable interrupt and IRQF is used to indicate which interrupt is occurred. If the specific IRQM doesn't enable then the hardware interrupt would not occurred. But the IRQF will response the status no matter how IRQM enable or not. For example, user enable TM2 to start counting. If IRQM bit 2 is enabled, the hardware interrupt would generate when timer overflow and IRQF bit 2 will be set. At the same time, program will jump to interrupt vector. User should clear IRQF in interrupt service routine, otherwise the interrupt would not work properly. Another condition is if IRQM bit 2 is disabled, the interrupt would not generate when timer overflow, but IRQF bit 2 still will be set. Program would not jump to interrupt vector.

IRQM ($31h)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRQM	INTM	PAM	PINTM	2HZM	PHM	TM3M/ PWM3M/ CAPT3M/ RFC3M	TM2M/ PWM2F/ CAPT2M/ RFC2M	TM0M/ TONEM

- Bit7 (INTM): Global enable/disable bit.
  - 0: Disable. All interrupts are mask.
  - 1: Enable. All interrupt are unmask

<Note> When interrupt is serving, the INTM will reset to "0" to prevent the other interrupt happen. After served, the RETI instruction will set INTM as '1'.

CPU_RESUME ($30h)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CPU_RESUME		PAR	PINTR	2HZR	PHR	TM3R/ PEM3R/ CAPT3R/ RFC3R	TM2R/ PWM2R/ CAPT2R/ RFC2R	TM0R/ TONER

- Bit7~0 : halt release mode control
  - 0: Disable.
  - 1: Enable.

CPU_RESUME	IRQM	Interrupt	Interrupt flag	Normal mode	HALT mode	SLEEP mode
1	X	Disable	V	Next command	1.wake-up system clock 2.Next instruction	Can't use
0	1	V	V	Jump 004h	1.wake-up system clock 2.LCALL 004h (Enter IRQ)	1.wake-up system clock 2.LCALL 004h (Enter IRQ)
0	0	X	V	X	No IRQ & No wake-up function	No IRQ & No wake-up function

IRQF ($32h)

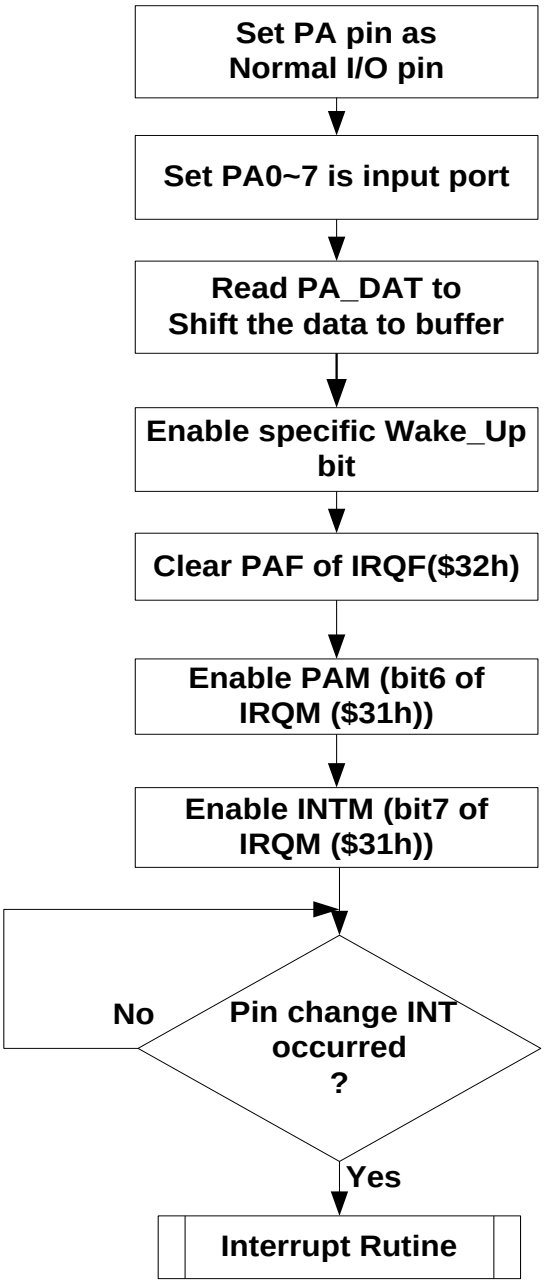
Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRQF		PAF	INTF	2HZF	PHR	TM3F/ PWM3F CAPT3F/ RFC3F	TM2F/ PWM2F/ CAPT2F/ RFC2F	TM0F/ TONEF

- Bit6 (PAF): PA0~7 Interrupt request flag: (pin-change)
  - 0: PA interrupt request off
  - 1: PA interrupt request on
- Bit5 (INTF): INT pin interrupt request flag:
  - 0: INT pin interrupt request off
  - 1: INT pin interrupt request on
- Bit4 (2HZF): 2HZ Interrupt request flag
  - 0: 2HZF overflow interrupt request off
  - 1: 2HZF overflow interrupt request on
- Bit3 (PHF): PH Interrupt request flag
  - 0: PH overflow interrupt request off
  - 1: PH overflow interrupt request on
- Bit2 (TM3F/PWM3F/CAPT3F/RFC3F): TM3 interrupt request flag
  - 0: TM3 overflow interrupt request off
  - 1: TM3 overflow interrupt request on
- Bit1 (TM2F/PWM2F/CAPT2F/RFC2F): TM2 interrupt request flag
  - 0: TM2 overflow interrupt request off
  - 1: TM2 overflow interrupt request on
- Bit0 (TM0F/TONEF): TM0/Capture Interrupt flag
  - 0: TM0 overflow or Tone interrupt request off
  - 1: TM0 overflow or Tone interrupt request on

External Interrupt Pin – PA[0~7] & PD[5]

4.5.1 PA Pin-change wake-up

Port A (PA[0~7]) provide external interrupt and wake up function. When device is not in sleep mode, the PA input single will serve as external interrupt. When external interrupt is occurred, program will jump to 004H (Interrupt vector). If device is in sleep mode, the PA input single will serve as wake up function. When wake up single input, device will let system clock work at first. Then wait for about 20mS wake up time. After that, program will jump to 004H. The below flow chart describe how to set port A to work as external interrupt or wake up function.



4.5.2 PA Key wake-up

Port A (PA[0~6]) provide Low power KEY wake up function.

There have 3 mothods for KEY function.Please refer to 4.3 KEY Strobe function

4.5.3 PD[5] edge wake-up

Port D (PD[5]) provide external interrupt and wake up function .

Bit5 of PAD_CTL3 would control rising or falling interrupt wake-up.

Please refer to 4.2-1 PD[5] wake-up function & PAD_CTL3.

Resister to Frequency Converter (RFC)

RFC is a kind of single slope integral circuit which can be used like low speed of 16 bit ADC to detect some resistor type sensor. MK9A35P has one set of RFC channels which have many different connections by setting register.

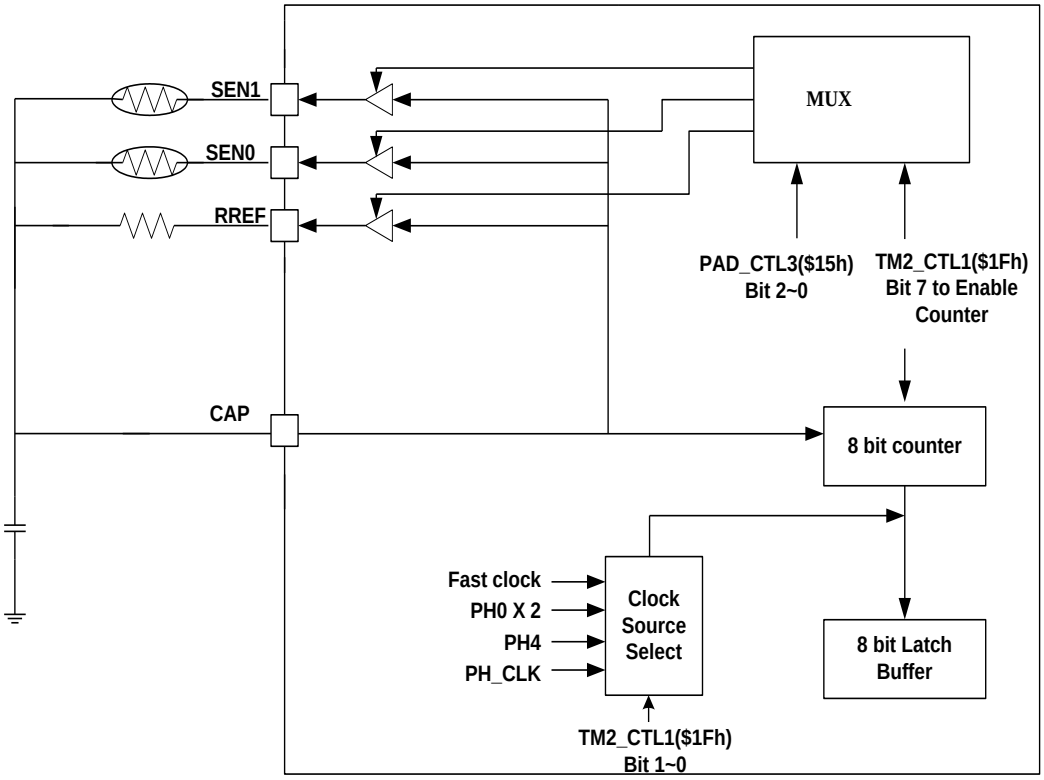


Fig.4.5.1 RFC application Block Diagram

One set of RFC block was composed of four external pins which are:

RREF: Reference resistor output pin

SEN0: Sensor 1 output pin

SEN1: Sensor 2 output pin

CAP: Oscillation input pin

Because all the RFC pins are shared with PA[0~3], user should set the specific register at first as below:

(a) TM2_CTL1 & TM2_CTL2 : 8/16-bit RFC mode

(b) Set bit5~0 of PAD_CTL2 ($14h) as (1,0,X,1,1,1). It means to set PA3~0 as RFC ports (RREF,SEN0,SEN1,CAP).

(c) Bit2~0 of PAD_CTL3($15h) : Control RREF,SEN0 & SEN1 ON/OFF

4.5.1 Timer 2 act as 8 bit Capture

This is one of the RFC 16 bit timer function. About setting flow, please refer to Fig.3.5.3. The source of 16 bit counter can be FCLK, PH0X2,PH4 or PH_CLK by setting RFC_CTL2 ($28h) bit2~1. CAPn input clock will be the event to latch the counter to latch buffer.

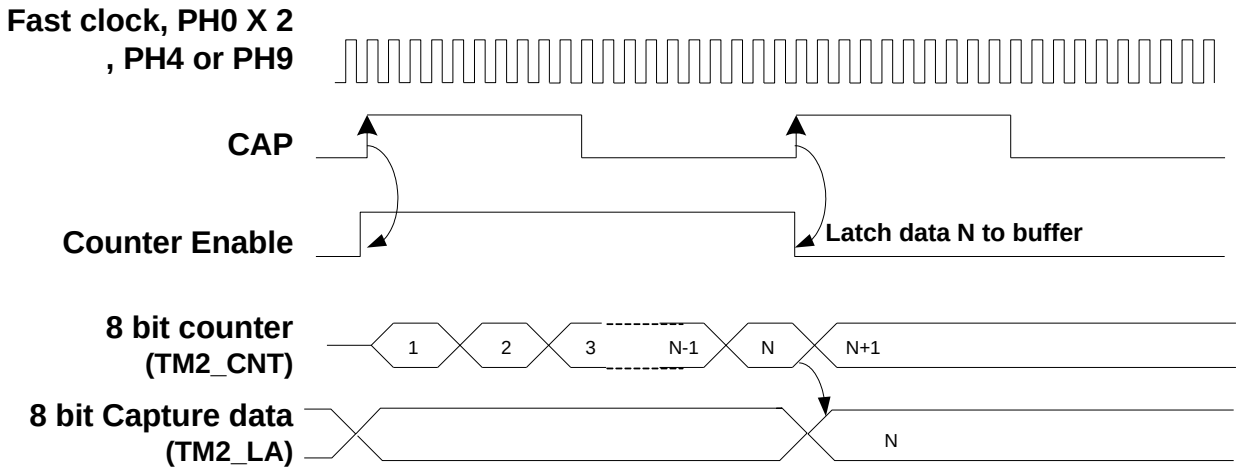


Fig.4.5.1 Timing Chart of RFC timer act as 8 bit Capture

4.5.2 Timer 2 act as RFC counter

When RFC timer act as 16 bit event counter to count the frequency of external RC oscillation, TM1 will be the time base and trigger signal to latch the data to buffer when timer overflow. The timing chart and setting flow are as below:

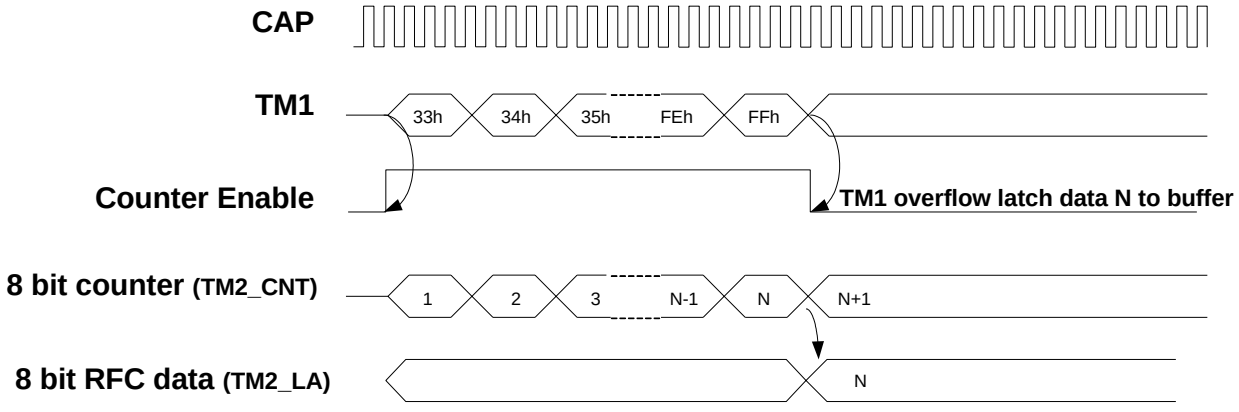


Fig.4.5.2 Timing Chart RFC timer act as RFC counter

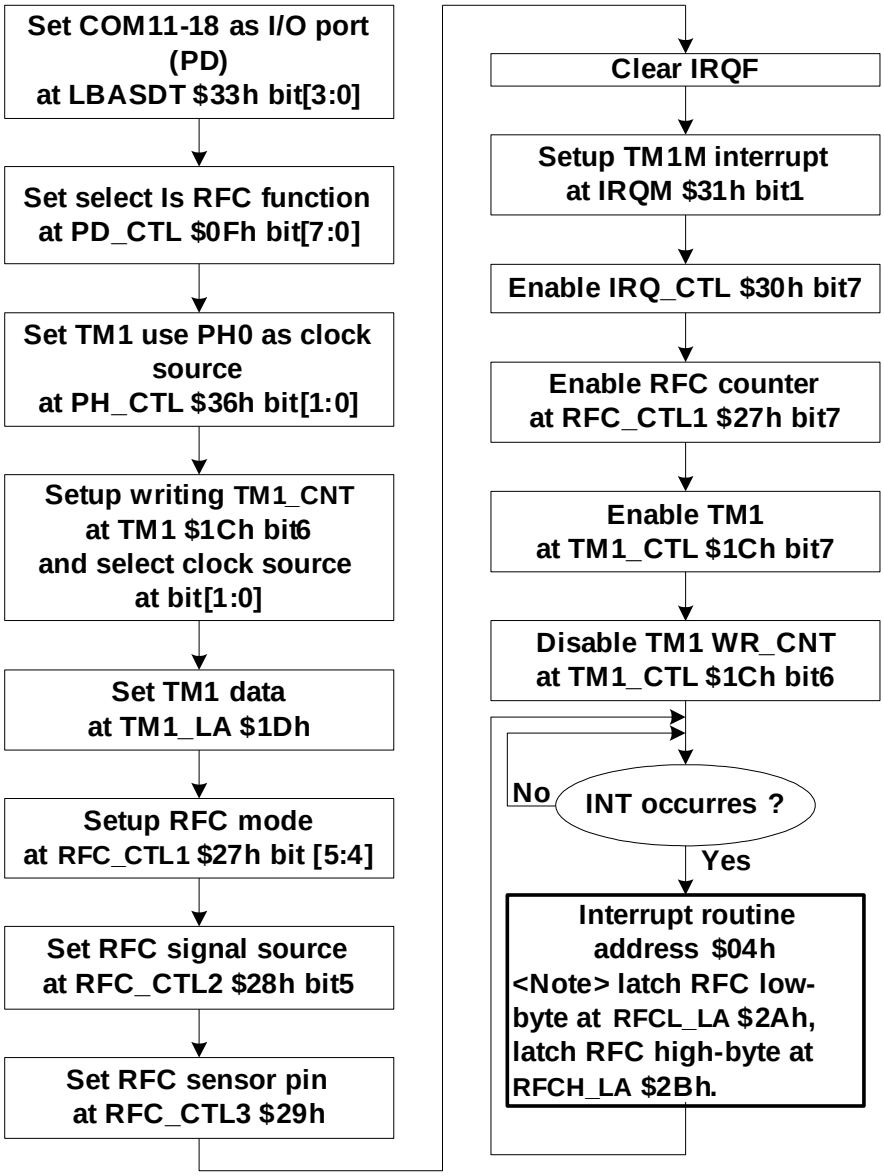


Fig.4.5.3 Setting Flow of RFC timer act as RFC counter

EL Panel Driver

MK9A35FP provide EL panel driver for LCD backlight. The application circuit is as Fig.4.6.1. Because the ELP/ELC pin are shared with SEG46~47, user should select the pin definition by setting SEG_CTL ($13h) at first.

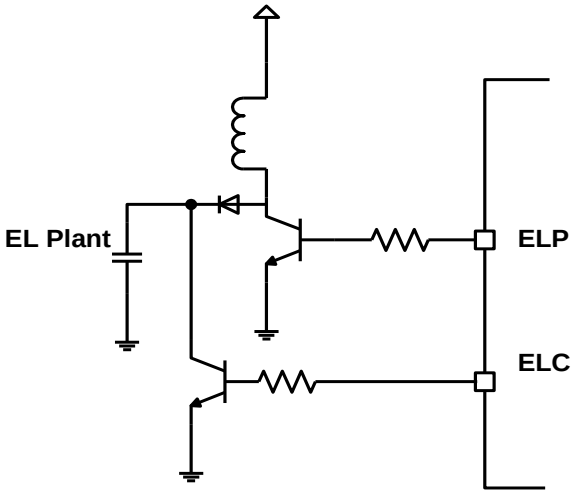


Fig.4.6.1 Application circuit of EL plant connection

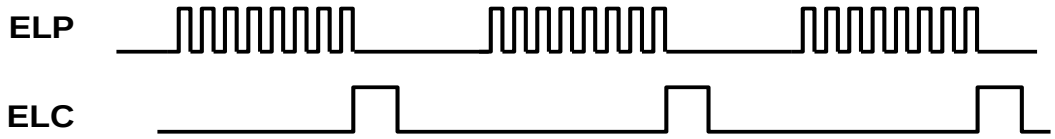


Fig.4.6.2 Timing Chart of EL Driver

PH_CTL ($36h) bit6~7 are used to control EL driver. Bit6 is used to set ELP/ELC pump frequency and duty as below table. Bit7 is used to turn on/off EL driver circuit.

Bit	Symbol	Description	
6	EL_SEL	1: Fast	ELP,ELC : High speed mode If Fast clock=500Khz: ELP: 15.6KHz , 15/16 duty ELC: 488Hz, 1/4 duty (L:H=3:1)
		0: Slow	ELP,ELC : Low speed mode if Slow clock=32Khz: ELP: 16KHz , 3/4 duty ELC: 512Hz, 1/4 duty (L:H=3:1)

Low Voltage Reset (LVR)

LVR function is used to prevent system from malfunction when the power drop to cause all the logics in unknown status. User can set different voltage or don't use this function by setting configuration register. The voltage in the table would have a little tolerance in different lot of chip and environment.

Bit7	Bit6	Detect voltage
LV1	LV0	
X	1	Don't use
1	0	1.9V
1	1	Don't use

Low Voltage Detect (LVD)

LVD function is used to detect battery low and prompt for user to change battery. User can set the detected voltage and status by SYS_CTL ($3Eh) bit4~3. This voltage in the table would have a little tolerance in different lot of chip and environment.

SYS_CTL ($3Eh)

Bit	Symbol	Description	
4~3	LVD1~0	Low voltage detector	
		1 1	ON (2.58V)
		1 0	ON (2.43V)
		0 1	ON (2.66V)
		0 0	Function OFF
2	LV	Low voltage detect output (read only)	
		1	VDD < 2.66V (or 2.43V,2.58V)
		0	VDD > 2.66V (or 2.43V,2.58V)

Other Register

PH_CTL ($36h):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH_CTL	ELON	EL_SEL	EL_P	CLR	PH_I1	PH_I0	PH_S1	PH_S0

- Bit7: This bit is to turn on/off EL light charge pump wave form
  0: ELP/ELC ON
  1: ELP/ELC OFF, the output signal will be low.

- Bit6: EL light charge pump wave form control

Bit	Symbol	Description	
6	EL_SEL	1: Fast	ELP,ELC : High speed mode If Fast clock=500Khz: ELP: 15.6KHz , 15/16 duty ELC: 488Hz, 1/4 duty (L:H=3:1)
		0: Slow	ELP,ELC : Low speed mode If Slow clock=32Khz: ELP: 16KHz , 3/4 duty ELC: 512Hz, 1/4 duty (L:H=3:1)

- Bit5: EL pad control

Bit \value	11	1X	01	00
(PH_CTL.EL_P),B6	Don"t use	ELP	SEG26	PD6
(PH_CTL.EL_P),B7	Don"t use	ELC	SEG27	PD7

1 : Clear PH11~PH15 and auto clear BIT5 (CLR) to "0".

- Bit4: Clear divider PH11~PH15

  0 : No clear

  1 : Clear PH11~PH15 and auto clear BIT5 (CLR) to "0".

- Bit3~2: PH IRQ (PHF) source select

Bit	Symbol	Description	
3~2	PH_I1~0	PH_I1~0	PH IRQ source select
		0 0	PHR <= PH10 (32hz)
		0 1	PHR <= PH11 (16hz)
		1 0	PHR <= PH12 (8hz)
		1 1	PHR <= PH13 (4hz)

- Bit1~0: (PH_CLK) PH source select

Bit	Symbol	Description	
1~0	PH_S1~0	PH_S1~0	PH_CLK
		0 0	PH_CLK <= PH9 (64hz)
		0 1	PH_CLK <= PH7 (256hz)
		1 0	PH_CLK <= PH8 (128hz)
		1 1	PH_CLK <= PH10 (32hz)

5. LCD Driver

MK9A35FP has maximum 189 segment (7com * 27seg). There are 1/2, 1/3, 1/4, 1/5, 1/6 and 1/7 Duty can be selected. Many COM pins are shared with I/O port or some special functions which let it more flexibility. If use less COM pin then the rest COM pin can be set to other function.

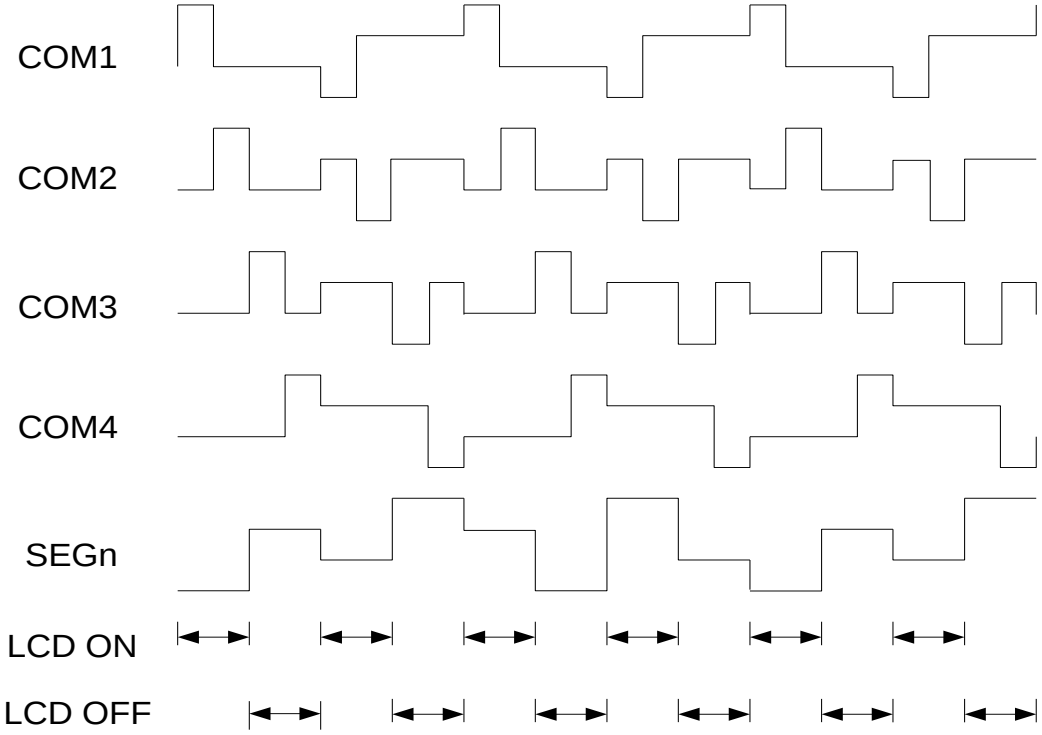


Fig.5.1.1-1 1/3 BIAS, 1/4 DUTY LCD ON/OFF waveform

5.1 LCD Pad Connections

MK9A35P has different kinds of power mode, duty, bias composition. The pad connection of different bias is not the same which is as below diagram:

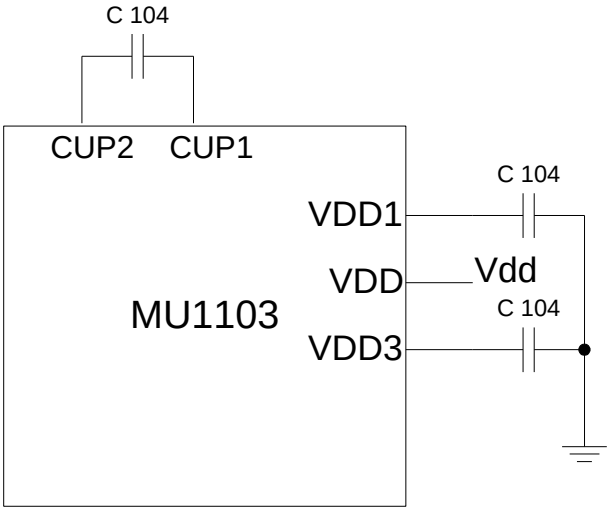


Fig.5.1.1-2 LI mode, (when VDD=3V , VDD=1.5V & VDD3=4.5V)

5.2 LCD Attribute Setting

There are many registers to set LCD driver attribute that is listed as below:

5.2.1 Bias Setting

Bias setting is in configuration register stage. Once it was fixed, user can not change by software.

5.2.2 Duty (COM) and Frame Frequency Setting

LBASDT ($33h) is used to set duty and LCD frame frequency. Once the duty is set which means the selected pin will be used as LCD COM output. The rest COM pin will automatically been a I/O ports. The register definition is as below:

LBASDT($33h): LCD DUTY SELECT (R/W)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LBASDT	LCD1	LCD0	FRAM1	FRAM0	--	LDUTY2	LDUTY1	LDTUY0

- Bit 7~6 : LCD1~0 mode select

  1 1 : LED mode 1 – COMn is high active , SEGn is low active

  1 0 : LED mode 2 – COMn is low active , SEGn is low active

  0 1 : LCD mode 2– don"t use

  0 0 : LCD mode 1– 1/3 bias charge pump .

MODE	LCD ON		LCD OFF	
	COMn	SEGn	COMn	SEGn
LCD1	4.5V / 0V	0V / 4.5V	0	0
LED1	VDD	0	0	0
LED2	0	0	VDD	0

	LCD OFF	ALL ON	LCD ON	ALL OFF
LCD1	V	V	V	V
LED1	V	X	V	X
LED2	V	X	V	X

- Bit5~4: LCD frame control (Write only)

  0 0 : FRAME 1

  0 1 : FRAME 2

  1 0 : FRAME 3

  1 1 : FRAME 4

DUTY	LCD FRAME (Hz)			
	FRAME 1	FRAME 2	FRAME 3	FRAME 4
1/2	58.14	43.48	87.41	115.7
1/3	56.82	42.74	85.62	114.7
1/4	56.82	42.74	85.62	114.7
1/5	57.47	43.10	86.81	113.6
1/6	56.82	42.74	85.62	114.7
1/7	60.24	43.48	90.58	117.9

DUTY	LED FRAME (Hz)			
	FRAME 1	FRAME 2	FRAME 3	FRAME 4
1/2	130.72	87.14	174.30	261.44
1/3	128.10	85.33	170.66	256.20
1/4	128.10	85.33	170.66	256.20
1/5	129.36	86.24	172.46	258.72
1/6	128.10	85.33	170.66	256.20
1/7	124.08	82.72	165.44	248.16

<Note> This frequency table base on 32KHz source clock. If user choose fast only clock mode and the clock is not 32KHz, the frequency would not be as above.

- Bit3~0: LCD driver duty setting (R/W)

LDUTY2	LDUTY1	LDUTY0	DUTY	COM 1~7	
				COM is for LCD	COM to be I/O
0	0	0	1/2	1~2	5~7
0	0	1	1/3	1~3	5~7
0	1	0	1/4	1~4	5~7
0	1	1	1/5	1~5	6~7
1	0	0	1/6	1~6	7
1	0	1	1/7	1~7	X
Others			Don't use		

5.2.3 LCD Pump Frequency and ON/OFF Control

LCD_CTL($35h): LCD Control (R/W) (default = 0000xx00b)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LCD_CTL	PUMP1	PUMP0	POW1	POW0	OVP1	OVP0	LCDM1	LCDM0

- Bit7~6 (PUMP1~0): LCD charge pump clock select.
  - 00: Original pump clock
  - 01: Original pump clock x 2
  - 10: don't use
  - 11: Original pump clock x 4
- Bit5~4 (POW1~0): Low speed power saving control (halt mode)
  - XX: default
- Bit3~2 (OVP1~0): LCD waveform control
  - 00: overlap
  - 01: $T_{NON\text{-}OVERLAP}$ (15uS)
  - 10: Reserved
  - 11: Reserved
- Bit1~0 (LCDM1~0): LCD mode select.

Bit1	Bit0	Mode	Status
0	0	Normal Mode	LCD power OFF
0	1	ALL ON Mode	When ALL ON is set to "0", all segment drivers are turned on waveform
1	0	Normal Mode	The display data in the register is output to the segment drivers LCD ON
1	1	ALL OFF Mode	When ALL OFF is set to "1", all segment drivers are turned off waveform

5.3 LCD Display RAM Mapping

The LCD driver has a LCD RAM. Each bit RAM map to specific COM/Segment as below table. If LCD RAM doesn't use, they can be used as working RAM to store data.

	Bit0~Bit6
	C1~C7
SEG1	$40
SEG2	$41
SEG3	$42
SEG4	$43
SEG5	$44
SEG6	$45
SEG7	$46
SEG8	$47
SEG9	$48
SEG10	$49
SEG11	$4A
SEG12	$4B
SEG13	$4C
SEG14	$4D
SEG15	$4E
SEG16	$4F
SEG17	$50
SEG18	$51
SEG19	$52
SEG20	$53
SEG21	$54
SEG22	$55
SEG23	$56
SEG24	$57
SEG25	$58
SEG26	$59
SEG27	$5A

6. Typical Application Circuit

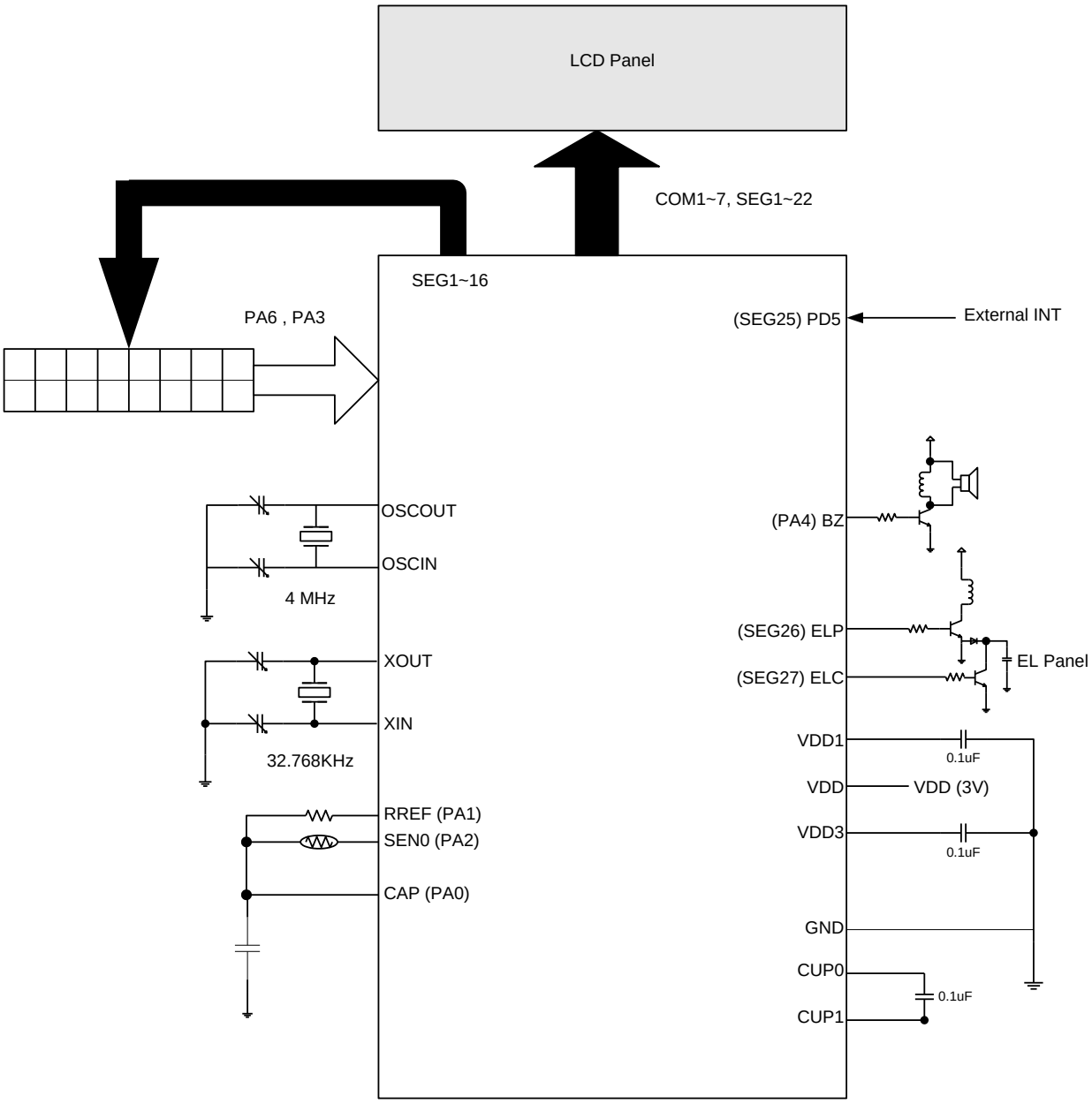


Fig.6.1 APPLICATION 1

7. Instruction Table

JUMP INSTRUCTION				
LCALL I	Call subroutine. However, LCALL can addressing 16K address	2	None	01ii iiii iiii iiii
LGOTO I	Go branch to any address	2	None	00ii iiii iiii iiii
LOGIC				
AND M, a	(M) · (acc) → (acc)	1	Z	1010 1000 MMMM MMMM
AND M, m	(M) · (acc) → (M)	1	Z	1010 1001 MMMM MMMM
ANDLA I	Immediate · (acc) → (acc)	1	Z	1111 1000 iiii iiii
COM M, a	~(M) → (acc)	1	Z	1010 0100 MMMM MMMM
COM M, m	~(M) → (M)	1	Z	1010 0101 MMMM MMMM
IOR M, a	(M) or (acc) → (acc)	1	Z	1011 1110 MMMM MMMM
IOR M, m	(M) or (acc) → (M)	1	Z	1011 1111 MMMM MMMM
IORLA I	Immediate or (acc) → (acc)	1	Z	1111 0010 iiii iiii
RL M, a	Rotate left from m to acc m[6:0]→acc[7:1] m[7]→ acc[0]	1	None	1110 0000 MMMM MMMM
RL M, m	Rotate left from m to itself m[6:0]→m[7:1] m[7]→ m[0]	1	None	1110 0001 MMMM MMMM
RLC M, a	Rotate left from m to acc m[7]→c m[6:0]→acc[7:1] c→acc[0]	1	C	1110 0010 MMMM MMMM
RLC M, m	Rotate left from m to itself m[7]→c m[6:0]→m[7:1] c→m[0]	1	C	1110 0011 MMMM MMMM
SL0 M, a	Shift left from m to acc m[6:0]→acc[7:1] 0→acc[0]	1	None	1110 0100 MMMM MMMM
SL0 M, m	Rotate left from m to itself m[6:0]→m[7:1] 0→m[0]	1	None	1110 0101 MMMM MMMM
SL1 M, a	Shift left from m to acc m[6:0]→acc[7:1] 1→acc[0]	1	None	1110 0110 MMMM MMMM
SL1 M, m	Rotate left from m to itself	1	None	1110 0111 MMMM MMMM

	m[6:0]→m[7:1] 1→m[0]			
RR M, a	Rotate right from m to acc 0→acc[7] m[7:1]→acc[6:0]	1	None	1110 1000 MMMM MMMM
RR M, m	Rotate right from m to itself M[0]→m[7] m[7:1]→m[6:0]	1	None	1110 1001 MMMM MMMM
RRC M, a	Rotate right from m to acc m[0]→c, c→acc[7] m[7:1]→acc[6:0]	1	C	1110 1010 MMMM MMMM
RRC M, m	Rotate right from m to itself m[0]→c, c→m[7] m[7:1]→m[6:0]	1	C	1110 1011 MMMM MMMM
SR0 M, a	Rotate right from m to acc 0→acc[7] m[7:1]→acc[6:0]	1	None	1110 1100 MMMM MMMM
SR0 M, m	Rotate right from m to itself 0→m[7] m[7:1]→m[6:0]	1	None	1110 1101 MMMM MMMM
SR1 M, a	Rotate right from m to acc 1→acc[7] m[7:1]→acc[6:0]	1	None	1110 1110 MMMM MMMM
SR1 M, m	Rotate right from m to itself 1→m[7] m[7:1]→m[6:0]	1	None	1110 1111 MMMM MMMM
SWAP M, a	m[7:4] → acc[3:0] m[3:0] → acc[7:4]	1	None	1011 1100 MMMM MMMM
SWAP M, m	m[7:4] ←→ m[3:0]	1	None	1011 1101 MMMM MMMM
XOR M, a	(M) xor (acc) → (acc)	1	Z	1011 0110 MMMM MMMM
XOR M, m	(M) xor (acc) → (M)	1	Z	1011 0111 MMMM MMMM
XORLA I	Immediate xor (acc) → (acc)	1	Z	1111 1001 iiii iiii
MATHEMATICS				
ADD M, a	(M)+(acc) → (acc)	1	C, DC, Z	1010 1010 MMMM MMMM
ADD M, m	(M)+(acc) → (M)	1	C, DC, Z	1010 1011 MMMM MMMM
ADDC M,a	(M)+(acc) + (carry) → (acc)	1	C, DC, Z	1011 1010 MMMM MMMM
ADDC M,m	(M)+(acc) + (carry) → (M)	1	C, DC, Z	1011 1011 MMMM MMMM
ADDLA I	Immediate + (acc) → (acc)	1	C, DC, Z	1111 1010 MMMM MMMM

BC M, bn	Clear bit n of (M)	1	None	1001 1bbb MMMM MMMM
BS M, bn	Set bit n of (M)	1	None	1001 0bbb MMMM MMMM
CLRA	Clear accumulator	1	Z	1010 0010 0000 0000
CLR M	Clear memory M	1	Z	1010 0011 MMMM MMMM
TABRDL M	Read low byte ROM table to (acc) ROM table address={TB_BNK,index of M }	2	None	1101 1000 MMMM MMMM
TABRDH M	Read high byte ROM table to (acc) ROM table address={TB_BNK,index of M }	2	None	1101 1001 MMMM MMMM
SUBC M, a	(M)+(/acc)+ (carry) → (acc)	1	C, DC, Z	1101 0100 MMMM MMMM
SUBC M, m	(M)+(/acc) + (carry)→ (M)	1	C, DC, Z	1101 0101 MMMM MMMM
DAA M, a	Decimal Adjust M to ACC If ACC[3:0] > 9 or DC=1 Then ACC[3:0]←ACC[3:0]+6, DC1=~DC else ACC[3:0] ←ACC[3:0], DC1=0 If ACC[7:4]+DC1 > 9 or C=1 Then ACC[7:4]←ACC[7:4]+6+DC1, C=1 else ACC[7:4] ←ACC[7:4]+DC1, C=C	1	C	1101 0110 MMMM MMMM
DAA M, m	Decimal Adjust M to memory If ACC[3:0] > 9 or DC=1 Then M[3:0]←ACC[3:0]+6, DC1=~DC else M[3:0] ←ACC[3:0], DC1=0 If ACC[7:4]+DC1 > 9 or C=1 Then M[7:4]←ACC[7:4]+6+DC1, C=1 else M[7:4] ←ACC[7:4]+DC1, C=C	1	C	1101 0111 MMMM MMMM

DAS M, a	Decimal Adjust M to ACC
	If ACC[3:0] > 9 or DC=0
	Then
	ACC[3:0]←ACC[3:0]-6,
	DC1=~DC
	Else
	ACC[3:0]←ACC[3:0], DC1=1
	If ACC[7:4] –DC1> 9 or C=0
	Then
	ACC[7:4]←ACC[7:4]-6-DC1,
	C=0
	else
	ACC[7:4] ←ACC[7:4]-DC1,
	C=~C
		1	C	1101 1110 MMMM MMMM

DAS M, m	Decimal Adjust M to memory If ACC[3:0] > 9 or DC=0	1	C	1101 1111 MMMM MMMM

	Then M[3:0]←ACC[3:0]-6, DC1=~DC else M[3:0] ←ACC[3:0], DC1=1 If ACC[7:4]-DC1 > 9 or C=0 Then M[7:4]←ACC[7:4]-6-DC1, C=1 else M[7:4] ←ACC[7:4]-DC1, C=C			
DEC M, a	(M) - 1 → (acc)	1	Z	1010 1100 MMMM MMMM
DEC M, m	(M) - 1 → (M)	1	Z	1010 1101 MMMM MMMM
INC M, a	(M) + 1 → (acc)	1	Z	1011 0000 MMMM MMMM
INC M, m	(M) + 1 → (M)	1	Z	1011 0001 MMMM MMMM
MOVAM m	(acc) → (M)	1	None	1010 0001 MMMM MMMM
MOV M, a	(M) → (acc)	1	Z	1010 0110 MMMM MMMM
MOV M, m	(M) → (M)	1	Z	1010 0111 MMMM MMMM
MOV2 M, a	(M) → (acc)	1	None	1111 0110 MMMM MMMM
MOV2 M, m	(M) → (M)	1	None	1111 0111 MMMM MMMM
MOVLA I	Immediate data → acc	1	None	1111 0000 iiii iiii
SUBLA I	(immediate data)-(Acc)→(Acc)	1	C, DC, Z	1111 0100 iiii iiii
SUB M, m	(M)–(acc) → (M)	1	C, DC, Z	1011 0101 MMMM MMMM
SUB M, a	(M) –(acc) → (acc)	1	C, DC, Z	1011 0100 MMMM MMMM
OTHER OPERATION				
NOP	No operation	1	None	1111 1111 1111 1111
CLRWDT	Clear watch-dog register	1	$\overline{TO}$, $\overline{PD}$	1111 1111 1111 0000
RET	Return (for lcall instruction)	2	None	1111 1111 1111 0001
IRETI	Return and enable INTM(for IRQ)	2	None	1111 1111 1111 0010
IRET	Return (for IRQ)	2	None	1111 1111 1111 0011
SLEEP	Enter sleep (saving) mode	1	$\overline{TO}$, $\overline{PD}$	1111 1111 1111 0100
CONDITION OPERATION				
BTSC M, bn	If (bit n of (M))=0, skip next instruction	1 or 2	None	1000 1bbb MMMM MMMM
BTSS M, bn	If (bit n of (M))=1, skip next instruction	1 or 2	None	1000 0bbb MMMM MMMM
DECSZ M, a	(M) - 1 →(acc), skip if (acc) = 0	1 or 2	None	1010 1110 MMMM MMMM
DECSZ M, m	(M) - 1 → (M), skip if (M) = 0	1 or 2	None	1010 1111 MMMM MMMM
INCSZ M, a	(M) + 1 →(acc), skip if (acc) = 0	1 or 2	None	1011 0010 MMMM MMMM
INCSZ M, m	(M) + 1 → (M), skip if (M) = 0	1 or 2	None	1011 0011 MMMM MMMM
TMSS SAZ	If (acc) =0, skip next instruction	1 or 2	None	1011 1000 XXXX XXXX
TMSC M SMZ M	If (M) = 0, skip next instruction	1 or 2	None	1011 1001 MMMM MMMM

TMSNC M SMNZ M	If (M) =\= 0, skip next instruction	1 or 2	None	1101 1011 MMMM MMMM
TMSNS SANZ	If (acc) =\=0, skip next instruction	1 or 2	None	1101 1010 XXXX XXXX
TMSNC M SMNZ M	If (M) =\= 0, skip next instruction	1 or 2	None	1101 1011 MMMM MMMM
TMSNS SANZ	If (acc) =\=0, skip next instruction	1 or 2	None	1101 1010 XXXX XXXX
TMCOMPE AMSE	If (acc) =(M), skip next instruction	1 or 2	None	1010 0000 MMMM MMMM
TMCOMPEB AMSNE	If (acc) =\=(M), skip next instruction	1 or 2	None	1101 1101 MMMM MMMM

8. Electrical Characteristis

8.1 Absolute Maximum Ratings

Supply Voltage …. Vss-0.3V to Vss+5.5V Storge Temperature ……. –50℃ to 125℃

Input Voltage …… Vss-0.3V to VDD+0.3V Operating Temperature… – 20℃ to 70℃

<Note>： These are stress ratings only. Stresses exceeding the range specified under"Absolute Maximum Ratings"may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

8.2 DC Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		VDD	Conditions				
VDD	Operating Voltage	---		2.2		3.6	V
I_{DD1}	Operating Current (32K Crystal)	3V	sleep mode, watchdog is off		1		uA
I_{DD2}	Operating Current (32K Crystal)	3V	sleep mode, watchdog is on		5.0		uA
I_{DD3}	Operating Current (32K Crystal)	3V	Halt mode,LCD is off, watchdog is off		4.6		uA
I_{DD4}	Operating Current (32K Crystal)	3V	Halt mode,LCD is off, watchdog is on		9.6		uA
I_{DD5}	Operating Current (32K Crystal)	3V	Halt mode,LCD is on, watchdog is off		5.5		uA
I_{DD6}	Operating Current (32K Crystal)	3V	Halt mode,LCD is on, watchdog is on		10.5		uA
I_{DD7}	Operating Current (32K Crystal)	3V	Halt mode,LCD is on, Hardware key sacn		10.5		uA
V_{IH1}	Port PA0~6	3V	Input Low to High Voltage		1.7		V
V_{IL1}	Port PA0~6	3V	Input high to Low Voltage		1.2		V
V_{IH2}	RESETB	3V	Input Low to High Voltage		1.5		V
V_{IL2}	RESETB	3V	Input high to Low Voltage		0.9		V
V_{IH3}	Port PC0~4	3V	input Low to High Voltage		1.6		V
V_{IL3}	Port PC0~4	3V	Input high to Low Voltage		1.2		V
V_{IH4}	Port PD0~7	3V	input Low to High Voltage		1.6		V
V_{IL4}	Port PD0~7	3V	Input high to Low Voltage		1.2		V

I_{IL}	Input Leakage Current	3V	Vin=VDD, VSS			1	μA
R_{PH1}	Pull-high Resistance	3V	Port PA0~6		227		Kohm
R_{PL1}	Pull-down Resistance	3V	Port PA0~6		280		Kohm
R_{PL2}	Pull-down Resistance	3V	Port PA7		440		Kohm
R_{PL3}	Pull-down Resistance	3V	Port PC0~2		93		Kohm
R_{PL4}	Pull-down Resistance	3V	Port PC3~4		280		Kohm
R_{PL5}	Pull-down Resistance	3V	Port PD0~7		93		Kohm
I_{LVR}	LVR Current	3V	Low Voltage Reset Config bit7.bit6=10		1.0		uA
V_{LVR}	LVR voltage	3V	Low Voltage Reset Config bit7.bit6=10		1.8		V
V_{LVD1}	LVD voltage	3V	SYS_CTL bit4.3=01		2.66		
V_{LVD2}	LVD voltage	3V	SYS_CTL bit4.3=10		2.43		
V_{LVD3}	LVD voltage	3V	SYS_CTL bit4.3=11		2.58		

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		VDD	Conditions				
I_{OH}	PA0~6 output port , PC0~4 output port, PD0~7 output port, Driving Current	3V	Voh=2.7V		1.8		mA
			Voh=2.4V		3.4		mA
			Voh=2.1V		4.6		mA
			Voh=2.1V		5.6		mA
I_{OL}	PA0~6 output port , PC0~4 output port, PD0~7 output port, Sink Current	3V	Voh=0.3V		6.6		mA
			Voh=0.6V		12		mA
			Voh=0.9V		15		mA
			Voh=1.2V		17		mA

8.3 AC Characteristics

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
		Conditions	VDD				
f_{sys1}	System Clock	LP Crystal mode	3V		32		Khz
f_{sys2}	System Clock	NT Crystal mode	3V	0.455		8	Mhz
f_{sys3}	System Clock	Internal 32K RC	3V		110		Khz
f_{sys4}	System Clock	Internal 500K RC	3V		580		Khz
f_{sys5}	System Clock	External fast RC	3V			4	Mhz
T_{wdt}	Watchdog Timer		3V		13		mS
T_{rht}	Reset Hold Time		3V		13		mS

8.4 External RC Table

Low speed external RC Table

R value	C value	RC frequency	R connect to (VDD,XIN)
110K	0.1u (suggest)	248 Khz	The capacitor is for stabile frequency
196K	0.1u (suggest)	118 Khz	
303K	0.1u (suggest)	68 Khz	
384K	0.1u (suggest)	53 Khz	
498K	0.1u (suggest)	40 Khz	
611K	0.1u (suggest)	30 Khz	

High speed external RC Table

R value	C value	RC frequency	R connect to (VDD,OSCIN)
298K	0.1u (suggest)	440 Khz	The capacitor is for stabile frequency
197K	0.1u (suggest)	640 Khz	
147K	0.1u (suggest)	840 Khz	
97K	0.1u (suggest)	1235 Khz	
50.3K	0.1u (suggest)	2.25 Mhz	
38.4K	0.1u (suggest)	2.95 Mhz	
29.4K	0.1u (suggest)	3.7 Mhz	

9.0 REVISION HISTORY

Document ID	Release date	Change notice
MK9a35fp v0.1	20140514	Datasheet release

10.0 Disclaimers

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