| 芯睿科技股份有限公司 mikkon technology limited | Total page | 10 |
|---|---|---|
| | Doc No | MK9A50P AP |
| | Rev. | 2.1 |

| 文件名稱 | MK9A50P 8 Bit Microcontroller AP Note |
|---|---|

| 版次 | 生效日 | ECN No. | 制修訂者 | 修訂內容概要 |
|---|---|---|---|---|
| 1.0 | | | 李崑旭 | 新頒。 |
| 1.1 | 99.1.7 | | Jemmy | P4 add. Comparator<br>P5 add. Power connect |
| 1.2 | 99.2.26 | | Jemmy | P6 1/2 Bias LCD |
| 1.3 | 99.3.16 | | Jemmy | P5. 補充說明 power connect |
| 2.0 | 2010.3.23 | | Jemmy | P7~10 Key , LCD & Idd |
| 2.1 | 2010.8.23 | | Jemmy | P9 2.40 < LCD < 2.75 |

| | | | | |
|---|---|---|---|---|
| | | | | |

# Table of Content

1. **MK9A50 更改 spec. (V16)**
   - **(1) 移除省電 (xin2,xout2)，將 (xin1,xout1) 放到 (xin2,xout2) 位置, VR2 改為 nc 腳 , SEG40~1 改為 SEG42~1**
   - **(2) SEG[41] & SEG[42]不用時, PC[4] & PC[3] 要設為 pull-down 才不會耗電**
   - **(3) PAD_CTL5 問題已修正 (spec. V24)**

**PAD_CTL5 ($28h): (R/W) (default =00000000b )**

| Register | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| PAD_CTL5 | -- | -- | -- | SEG23/ PC[6] | SEG24/ PC[7] | SEG42/ PC[3] | SEG41/ PC[4] | PWM3/ PD[3] |

2. **IRQF**

**IRQF 不要使用 BC instruction.**

**BC IRQF, 0 ➔ 除了清除 bit0，也可能誤清 別的 bit.**

**請使用**

**Movla b'11111110'**

**Movam IRQF ➔ 寫入 "1" 是 don't，並不真的寫 Hi，寫"0" 則清除.**

3. **(XIN1,XOUT1)**

(XIN1,XOUT1) 架構跟 MK9A35P (XIN,XOUT) 相同 .

C1 & C2 電容會影響耗電大小. (C1 & C2 越小越省電)

MK9A50P normal crtsatl 2hz halt mode Idd=1.7~1.8uA (XIN1 & XOUT1)

4. **ELC & ELP**

| Bit \value | 11 | 10 | 01 | 00 |
|---|---|---|---|---|
| (PH_CTL.EL_P),B6 | Do'nt | ELP | SEG39 | PD6 |
| (PH_CTL.EL_P),B7 | Do'nt | ELC | SEG40 | PD7 |

5. PD4 pull-down 設定問題

**PD_PUD ($10h) : (R/W) (default =00000000b )**

| Register | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **PD_PUD** | CD7 | CD6 | CD5 | CD4 | CD3 | CD2 | CD1 | CD0 |

**<Note> When these shared pins are set as PD, there are PMOS open drain or NMOS open drain can be selected. The setting method is as below table:**

**CD7 – PD7 pull down control**
**CD6 – PD6 pull down control**
**CD5 – PD5 pull down control**
**CD4 – don't care**
**CD3 – PD3 & PD4 pull down control**
**CD2 – PD2 pull down control**
**CD1 – PD1 pull down control**
**CD0 – PD0 pull down control**

| DDn (PD_DIR) | CDn | PULL-DOWN | PMOS OPEN-DRAIN | Description PDn (n=0,1,2,3,5) |
|---|---|---|---|---|
| 1 | 0 | OFF | OFF | PDn is input port |
| 1 | 1 | **ON** | OFF | PDn is input port |
| 0 | 0 | ON | ON | PDn is normal output |
| 0 | 1 | OFF | ON | PDn is pmos open drain output port |

| DDn (PD_DIR) | CDn | PULL-DOWN | PMOS OPEN-DRAIN | Description PDn (n=4) |
|---|---|---|---|---|
| 1 | CD4=0 | OFF | OFF | PDn is input port |
| 1 | CD4=1 | **OFF** | OFF | PDn is input port |
| 1 | CD3=1 | **ON** | OFF | PDn is input port |
| 0 | CD4=0 | ON | ON | PDn is normal output |
| 0 | CD4=1 | OFF | ON | PDn is pmos open drain output port |

# 6. Key matrix (MK9A35E,MK9A50 & MK9A80 & MK9A160)

| | *MK9A50* | *MK9A35EP* | *MK9A80* | *MK9A160* |
|---|---|---|---|---|
| *STROBE* | *(1)* | *(2)* | *(2)* | *(2)* |
| *I/O pull-down* | *100K* | *100K* | *100K* | *100K* |
| *Key strobe Pull-down* | *100K* | *10K* | *10K* | *100K* |

## 6.1 STROBE(1)

**MK9A50 : STROBE($34h)**

| Register | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **STROBE** | KIEN1 | KIEN0 | KOAEN | KOEN | KO3 | KO2 | KO1 | KO0 |

- Bit7~6 (KIEN1~0): Key mode select

| Bit \value | 11 | 10 | 01 | 00 |
|---|---|---|---|---|
| KIEN1~0 | Hardware mode 2 | Hardware mode 1 | Software mode | OFF |

| MODE/FUNCTION | SEG1~16 | PORT PA0~6 & PC0~7 | PORT PD3~4 | IRQ |
|---|---|---|---|---|
| Hardware mode 2 | X | Pull down enable | X | V |
| Hardware mode 1 | Hi output | Pull down enable | X | V |
| Software mode | X | Pull down enable | Pull down enable | X |
| KOAEN | SEG1~16 : Hi output | X | X | X |
| KOEN | SEGn : Hi output<br>Others : Floating | X | X | X |

**(1)省電. 有 IRQ 可以使用**

**(2)Key (or I/O ) Pull-down resister =100K**

## 6.2 STROBE(2)

**MK9A35E/MK9A80/MK9A160 STROBE ($34h)**

| Register | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **STROBE** | FRAME | EN | KOAEN | KOEN | KO3 | KO2 | KO1 | KO0 |

| MODE/FUNCTION | SEG1~16 | PORT PD[0~7] & PC[0:1] | PORT PA[0~6] |
|---|---|---|---|
| EN | X | Pull down enable | Can't connect to SEGn |
| KOAEN | SEG1~16 : Hi output | X | X |
| KOEN | SEGn : Hi output<br>Others : Floating | X | X |

**(1) Bit7 Frame : read only**

**(2) Software mode only**

**(3) Frame=1 時, 讀 key 會比較省電**

**(3) Mk9A35E/MK9A80 :Key Pull-down=10K,**
**I/O pull-down=100K**

當 **key** 的內阻大於 **2K** 時,會認不到 **key.**

**(4)Mk9A160 :Key Pull-down & I/O pull-down=100K**

## 7. **LCD/LED** (MK9A35E,MK9A50 & MK9A80 & MK9A160)

| *LCD2~0* | *MK9A50* | *MK9A35EP* | *MK9A80* | *MK9A160* |
|---|---|---|---|---|
| *X 0 0* | *1/3 bias* | *1/3 bias* | *1/3 bias* | *1/3 bias* |
| *X 0 1* | *Led 3* | *1/2 bias #* | *1/2 bias* | *1/2 bias* |
| *X 1 0* | *Led 2* | *Led 2* | *Led 2* | *Led 2* |
| *X 1 1* | *Led 1* | *Led 1* | *Led 1* | *Led 1* |
| *1 0 0* | *x* | *x* | *x* | *1/4 bias* |
| *Duty 1/N* | *4,5,6,7,8* | *2,3,4,5,6,7* | *2,3,4,5,6,7,8* | *2,3,4,5,6,7,8, 10,12,16* |

(1) MK9A35E/50/80 : 沒有 LCD2 這個 bit
(2) MK9A50 Led3 : ICE 上必須要放 100-pin MK9A50 display.
(3) MK9A35E 1/2 bias 波形與 MK9A80/160 不同,
某些玻璃會有殘影, 使用此功能必須使用 100-pin MK9A35E display.
(4) VDD2 接 VDD 時,
1/2 bias : VDD1=VDD/2 , VDD2=VDD3=VDD4=VDD
1/3 bias : VDD1=VDD/2 , VDD2=VDD, VDD3=VDD4=VDD *3/2
1/4 bias : VDD1=VDD/2 , VDD2=VDD, VDD3=VDD*3/2,
VDD4=VDD * 2.

## 8. **Idd (MK9A35E,MK9A50 & MK9A80 & MK9A160)**

省電模式的設定

| | *MK9A50* | *MK9A35EP* | *MK9A80* | *MK9A160* |
|---|---|---|---|---|
| *STATUS bit6* | *x* | *Bit6=1* | *Bit6=1* | *Bit6=1* |
| *LV* | *1.5,1.7& 2V* | *2V (fix)* | *2V (fix)* | *1.5,1.7& 2V* |
| *Config bit12* | *x* | *bit12=1* | *bit12=1* | *bit12=1* |
| *LCD_CTL bit5.4* | *Bit5.4=11* | *Bit5.4=11* | *Bit5.4=11* | *Bit5.4=11* |
| *Idd (no LVR)* | *2uA* | *--* | *--* | *1.1uA* |
| *Idd (include LVR)* | *2.3uA* | *1.7uA* | *1.4uA* | *1.4uA* |
| *LVR* | *0.3uA* | *0.3uA* | *0.3uA* | *0.3uA* |

## 9. *LVD (MK9A35EP,MK9A50P.MK9A80P,MK9A160P)*

2010.9 LVD 部分測試加測 2.56V 這一階, 範圍 2.45~2.70 不過考量儀表的誤差, spec. 範圍訂為 2.40~2.75V

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| $V_{LVD1}$ | LVD voltage | 3V | SYS_CTL bit4.3=01 | | 2.68 | | V |
| $V_{LVD2}$ | LVD voltage | 3V | SYS_CTL bit4.3=10 | | 2.42 | | V |
| $V_{LVD3}$ | LVD voltage | 3V | SYS_CTL bit4.3=11 | 2.40 | 2.56 | 2.75 | V |